ALVEO™ SN1000 SmartNICs

AMD
ALVEO
SN1000

OVERVIEW

The explosive growth of big data and increasing complexity in the modern data center demands hardware accelerators to offload a broad range of critical data center applications from CPUs. Cloud providers and enterprises must continually optimize for complex applications, adapt acceleration and resources across multiple workloads and deliver a broader range of offloads. These challenges require scalable, low-latency hardware acceleration while retaining rapid reconfigurability for changing and emerging workloads.

The Alveo™ SN1000 family of composable SmartNICs meets these challenges with software-defined hardware acceleration. Revolutionary Xilinx composability empowers providers and enterprises to effortlessly support new protocols, build custom offloads, and deploy efficient and fluid application-specific data paths using P4 or high-level synthesis (HLS).

SN1000 SmartNICs deliver protocol-level programmability at linerate performance, and are powered by a AMD 16nm UltraScale+™ architecture FPGA and an A72 Arm® processor subsystem with support for up to 16 cores.

Starting with the SN1022 100Gb/s composable SmartNIC, the Alveo™ SN1000 family provides a comprehensive suite of solutions for network, storage, and compute acceleration functions on a single platform.

> High Performance NIC - 100Gb connectivity with industryleading small packet performance and low-latency on PCIe Gen 4.

> Software Defined Infrastructure - Open Virtual Switch (OVS) and Virtio offloads with efficient switching and routing along with a powerful Arm A72 processor for bare metal services and control plane offloads.

> NFV Workload Acceleration – Decoupling of network functions and services from dedicated hardware for efficient and high performance acceleration.

> Security - Root-of-Trust secure boot and technology to ensure the integrity of the firmware and hardware.

> QoS – Support for traffic shaping and management mechanisms with dedicated independent queues in hardware.

> Programmability - P4 and HLS programming allowing the data plane to be fully software-defined for cloud-scale deployments.

AMD ADVANTAGE

> Fully composable and programmable

- Versatile solution for containerized, virtualized, bare metal deployments

- Comprehensive suite of security offloads including IPsec, kTLS, and SSL/TLS

- Storage acceleration for NVMe/ TCP, Ceph and services including compression and crypto

> Deploy hardware-accelerated custom plugins programmed in P4, HLS, or RTL

- Adapt to changing requirements without replacing hardware

> Hardware Root-of-Trust

Performance	SN1022
Full Duplex Throughput	200Gbps
Packet Rate	100Mpps
TCP Throughput	100Gbps
Latency (1/2 RTT)	<3us
OVS Performance[1]	100Gbps
Flow Table Entries	4M Stateful Connections
IPsec Encryption Throughput	100Gbps
Power	75W

FEATURES

Hardware

- PCIe Gen 4 x8 or Gen 3 x16
- 100G QSFP28 DA copper or optical transceiver
- XCU26 FPGA based on Xilinx 16nm UltraScale+ architecture
- On-board CPU: 16 64-bit Arm Cortex®-A72 cores at 2.0 GHz with 8 MB cache
- 1x 4GB x 72 DDR4-2666 (Processor)
- 2x 4GB x 72 DDR4-2666 (FPGA)

General Networking

- TCP/UDP Checksum Offload (CSO), TCP Segmentation Offload (TSO), Generic Send Offload (GSO)
- Generic Receive Offload (GRO), Receive Side Scaling (RSS)
- VLAN Insertion/Removal
- VLAN Q-in-Q Insertion/Stripping
- Jumbo Frames (up to 9KB)

Traffic Steering

- TCP/UDP/IP, MAC, VLAN, RSS filtering Accelerated Receive Flow Steering (ARFS), Transmit Packet Steering (XPS)

Virtualization

- Linux Multi-queue
- Single Root I/O Virtualization (SR-IOV)
- Tunneling offloads; adaptable to custom overlays.

Software and FPGA Extensibility

- Support for custom plug-ins to enable new functionality; programmed via P4, HLS, or RTL.

Manageability and Remote Boot

- UEFI
- Secure Firmware Upgrade and Hardware Root of Trust
- NC-SI, PLDM Monitoring and Control, PLDM Firmware Update and MCTP support
- MCTP transports support SMBus and PCIe VDM

OS Support

- Red Hat RHEL, CentOS, Ubuntu, SLES, Debian for Host CPU
- Debian-derived Linux distro for on-board Arm CPU

Network Acceleration

- Onload®/ TCPDirect - TCP/UDP
- Open Virtual Switch (OVS)
- DPDK Poll Mode Driver

Hardware Offloaded Virtio-net

- Virtio v0.9.5 and later
- CSO, TSO
- Multi-queue
- vDPA (Virtual Data Path Acceleration)

Hardware-based Packet Processing

- Wildcard match-action flow tables
- Tunnel encap/decap – VXLAN, NVGRE
- Connection Tracking
- Packet Replication
- Header rewrite/NAT
- Per-rule packet and byte counters
- MAC Address rewriting
- 4 M stateful connections and up to 20K Megaflows with wildcard match support

Storage Acceleration

- Ceph RBD Client Offload
- Hardware Offloaded Virtio-net

  - Virtio v0.9.5 and later
  - Multi-queue

Environmental Requirements[2]

- Temperature:

  - Operating: ≤ 30°C (86°F)
  - Storage: −40°C to 75°C (−40°F to 167°F)

- Humidity:

  - Operating: 8% to 90%, and a dew point of −12°C
  - Storage: 5% to 95%

Physical Dimensions (without bracket)

- Full Height Half Length PCIe CEM
- L: 6.59 inch (167.5 mm)
- W: 4.38 inch (111.15 mm)
- H: 0.72 inch (18.3 mm)

Ordering Information

- A-SN1022-P4N-PQ: Encryption Disabled
- A-SN1022-P4E-PQ Encryption Enabled

Take the Next Step

For more information, documents, and reference designs, or to purchase, visit **AMD Alveo SN1000 SmartNICs**

Notes:
Feature availability is software release dependent. Please check release notes or contact **AMD Support** for more information.
1. Performance is driver dependent. Please check release notes or contact Xilinx Support for more information.
2. Environmental specs are preliminary.

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