Teledyne e2v Develops High-Speed Data Conversion Platform to Accompany Latest Xilinx FPGAs

Grenoble, 20th April 2020 – In response to the ongoing advances in programmable logic technology, Teledyne e2v has made further enhancements to its portfolio of data converters, along with the high-speed SERDES technology that supports them.

Complementing the popular 20nm Kintex UltraScale KU060 FPGAs from Xilinx, Teledyne-e2v now offers highly optimized multi-channel analog-to-digital converter (ADC) and digital-to-analog converter (DAC) solutions. These are available in a variety of different grade classes - going all the way up to a robust, radiation-tolerant space version that is suitable for satellite communications, earth observation, navigation and scientific missions.

The new data converters are each able to interoperate with their associated FPGA through incorporation of a form of the ESIstream high-speed serial interface protocol that has been modified for use with the KU060 series. With a 12.5Gbps data rate supported, ESIstream delivers industry-leading operational parameters, in terms of both heightened data efficiency and shortened serial link latency levels. In addition, it facilitates the synchronization of multiple lanes and multiple devices.

Although ESIstream was originally developed by Teledyne-e2v engineers, the company is not looking to make it a proprietary protocol. Instead the objective is to encourage its widespread adoption in high-performance FPGA system designs - so that elevated sampling rates can be supported, while still keeping the firmware overhead involved to a minimum. ESIstream is available license-free, with customers able to download the related code and then make alterations to it in order to fit their own specific requirements (such as enhanced redundancy mechanisms, etc.).

The effectiveness of Teledyne e2v data conversion platform in conjunction with the KU060 FPGA series has been thoroughly tested. This has been undertaken by Teledyne e2v engineers using the ADA-SDEV-KIT2 evaluation board from Alphadata, another key Xilinx ecosystem partner, using 8 lanes of ESIstream.

"The space-constrained nature of modern high-density hardware deployments means that the area of programmable logic fabric allocated to serial interfacing needs to be reduced" explains Stéphane Breysse, Product Applications Engineer - FPGA Interfaces at Teledyne e2v Semiconductors. "This is why the ESIstream IP is such a valuable addition to our overall data conversion offering. It enables greater degrees of optimization to be realized and makes

better use of available programmable logic assets, while also achieving superior reliability characteristics."

About Teledyne e2v

Teledyne e2v's innovations lead developments in healthcare, life sciences, space, transportation, defence and security and industrial markets. Teledyne e2v's unique approach involves listening to the market and application challenges of customers and partnering with them to provide innovative standard, semi-custom or fully-custom solutions, bringing increased value to their systems.

Website: www.teledyne-e2v.com/products/semiconductors

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