SPACE-GRADE FPGAS

Challenges of High-Performance Electronic Systems in Space

- Achieving high performance and integration without incurring the costs, risk, and long development times of ASICs
- Implementing hardware changes late in the design cycle
- Ensuring reliable operation in high-radiation environments

The Xilinx Radiation-tolerant Virtex-4QV FPGA Family Solution

- Reconfigurable technology enables hardware design changes at any time
- Multiple sub-families provide high-performance and advanced capabilities while eliminating non-recurring engineering (NRE) expenses
- Single-chip solution for embedded computing, signal processing, communications, and control functions
- Guaranteed radiation tolerance for space applications

XILINX
ALL PROGRAMMABLE™

SPACE-GRADE RADIATION-TOLERANT VIRTEX-4QV FPGAs

Xilinx® space-grade FPGAs offer a compelling alternative to ASIC and other one-time programmable logic technologies. The Virtex®-4QV family provides three domain-specific, radiation-tolerant sub-families, with different mixes of capabilities:

- LX: High-performance logic
- SX: Ultra-high performance signal processing
- FX: Embedded processing

Large-Capacity System Integration and High-Performance in Space

Building on the Xilinx legacy of space-grade reconfigurable FPGAs established with the Virtex and Virtex-II families, the Virtex-4QV family delivers exceptional levels of integration and performance. These devices meet the requirements of demanding applications including video, communications, radar, packet processing, and encryption.

Xilinx Virtex-4QV devices offer up to 200,000* logic cells, 10Mbit of RAM/FIFO, two built-in PowerPC® 405 processor blocks with an APU controller, 512 DSP™ slices, and four built-in Ethernet blocks. Virtex-4QV FPGAs deliver outstanding performance with 400MHz clocking, DSP slices delivering 204 GMACs at 400MHz, and 350MHz PowerPC processors, all in a single device. Flexible 800 Mbps differential I/O and 500 Mbps single-ended I/O support industry-standard and custom protocols. The APU controller in the PowerPC processor block makes it easy to integrate custom offload hardware to boost processing performance.

Special processing combined with SEE mitigation techniques and tools make it possible for aerospace designers to take advantage of all the benefits of high-performance, high-density FPGA technology. In-system reconfiguration enables engineers to make hardware design changes to enhance system functionality at any time, even after launch.

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe

Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

India

Meenakshi Tech Park
Block A, B, C, 8th & 13th floors,
Meenakshi Tech Park, Survey No. 39
Gachibowli(V), Seri Lingampally (M),
Hyderabad -500 084
Tel: +91-40-6721-4000
www.xilinx.com

Guaranteed Radiation Tolerance

Virtex-4QV FPGAs are guaranteed for total high level ionizing dose and single-event latch-up immunity. Xilinx pioneered the application of SRAM-based FPGAs in high-radiation environments and together with JPL founded the Xilinx Radiation Test Consortium to conduct single-event upset (SEU) characterization and report the results. To review Consortium findings, visit:
http://parts.jpl.nasa.gov/organization/group-5144/radiation-effects-in-fpgas/xilinx/

- Total Ionizing Dose – Xilinx tests each wafer lot per Method 1019 to ensure that device performance meets or exceeds the guaranteed DC electrical specification requirements, as well as AC and timing parameters at 300 krad (Si).

- Single-Event Latchup – The radiation-tolerant Virtex-4QV technology incorporates a thin epitaxial layer in the wafer manufacturing process for latch-up immunity. For each Virtex-4QV device type, the SEE consortium verified latchup immunity at maximum Vcc and operating temperature, subjected to a heavy ion fluence exceeding $1x10^7$ particles/cm^2, with linear energy transfer (LET) exceeding 125 MeV-cm^2/mg.

- Single-Event Upset – Xilinx conducted additional experiments in heavy ion, proton, and neutron environments in order to measure and document the susceptibility and consequence of SEU(s). The SEE Consortium oversaw and validated the test methods, empirical data collected, and resulting analysis. In conjunction with the SEE Consortium, Xilinx developed beam-tested, upset mitigation solutions. For mitigation, Xilinx provides triple modular redundant reference designs, configuration memory scrubbing application notes, and the TMRTool™ for automating error-free triplication of designs destined for space.

Widest Selection of IP and Tools

To help accelerate every phase of system design, Xilinx offers a complete development ecosystem that includes: ISE™ Design Suite, the award-winning FPGA design software that helps you achieve maximum performance and rapid timing closure; the EDK embedded development kit; ChipScope™ analyzer; a library of more than 600 proven IP cores; application notes; and Xilinx technical support.

* Radiation tolerance requires triple modular redundancy; the logic cell capacity, therefore, must take into account triplication of all inputs, feedback logic, and outputs, as well as the voters that must be inserted on feedback and output paths.

	VIRTEX-4QV FPGAS OPTIMIZED FOR:			
	LOGIC	DSP	EMBEDDED PROCESSING	
Part Number	XQR4VLX200	XQR4VSX55	XQR4VFX60	XQR4VFX140
Core Voltage	1.2V	1.2V	1.2V	1.2V
Slices	89,088	24,576	25,280	63,168
Logic Cells*	200,448	55,296	56,880	142,128
CLB Flip-Flops	178,176	49,152	50,560	126,336
Maximum Distributed RAM (Kb)	1,392	384	395	987
Block RAM/FIFO (18 Kb each)	336	320	232	552
Total Block RAM (Kb)	6,048	5,760	4,176	9,936
Digital Clock Manager (DCM)	12	8	12	20
Maximum Single-Ended I/Os	960	640	576	896
Maximum Differential I/O Pairs	480	320	288	448
Digitally Controlled Impedance	Yes	Yes	Yes	Yes
DSP Slices	96	512	128	192
10/100/1000 Ethernet MAC Blocks	—	—	4	4
PowerPC® Processor Blocks	—	—	2	2
Speed Grades	-10	-10	-10	-10
Configuration Memory (Mb)	51.4	22.7	21.0	47.9
Manufacturing Grades	V	V	V	V
Total Ionizing Dose (krad)	300	300	300	300
SEL Immunity (MeV-cm^2/mg)	>125	>125	>125	>125
Package / Area	Available User I/Os			
CFA Packages (CN): Flip-chip, ceramic column grid array (1.0 mm ball spacing)				
CN1144 35 x 35 mm			576	
CN1140 35 x 35 mm		640		
CN1509 40 x 40 mm	960			768

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