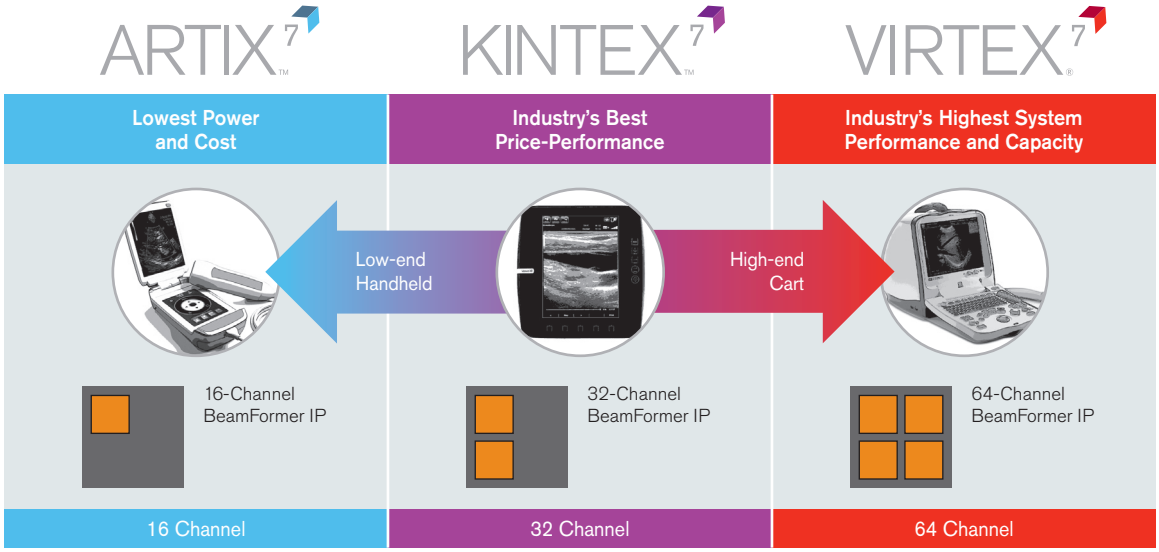
2010
INNOVATIONS

UNIFIED ARCHITECTURE

Industry's First Unified Architecture Fosters Quality Advancements

The new Xilinx 7 series families employ a *unified architecture,* providing unparalleled portability, scalability, and productivity. Devices in the three families are designed with the same architectural building blocks using the fourth-generation ASMBL™ architecture, including logic fabric (CLB and routing), block RAM, DSP slices, and clocking technology.



Repeatability

In the past, Xilinx products were designed uniquely for each silicon family. This required device-specific handling and processes throughout development. Beginning with the 7 series, Xilinx has adopted a reuse approach that leverages design blocks across the entire family. This approach has not only reduced complexity in terms of layout, simulation, characterization, test development, and reliability, but also streamlines activities that contribute to a more repeatable and reliable technology delivery process.

Enabling Higher-Quality Design Practices

A unified architecture, with common blocks across different FPGA families, allows specific development improvements that lower the customer risks associated with introducing new technology:

- *Better software models allowing shorter test development, unification, and characterization, resulting in better overall product performance*
- *Earlier and deeper silicon, software, and IP characterization*
- *Advanced, integrated quality testing on Targeted Design Platforms*

CONT'D. >>

Freeing Resources for Technology Development

The commonalities at the heart of the 7 series device families reduce the Xilinx resources and time required for many quality-centric processes. There are fewer blocks to design, lay out, verify, and implement in software and IP. Having fewer versions to validate frees up engineering resources, accelerating the new product evaluation and introduction (NPE/NPI) processes.

As a result, Xilinx has been able to shift more resources to quality advancements. This has been especially important for the introduction of 28nm devices, which require more stringent device modeling due to increased circuit sensitivity. Xilinx has been able to take a proactive approach in developing an improved 28nm test vehicle methodology:

- *Multiple test vehicles that incorporate structures to correlate silicon results against the device model and fine-tune the accuracy of the device model*
- *Optimized design/manufacturing interactions for yield, circuit marginality, sensitivity through design-for-manufacturability (DFM)*
- *Worst-case simulations applied at different levels of abstraction to minimize the impact of process variations on performance and other types of parametric yield loss*

In 2010, Xilinx quality engineering also increased investments in:

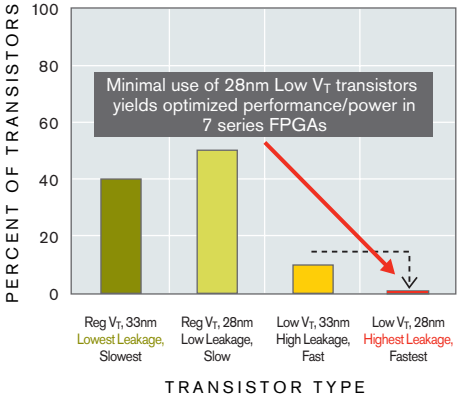
- *Design methodology, design-for-margin, and standardizing speed specification methods*
- *Improving device robustness and reliability*
- *Enhancing the intuitive design flow for improved ecosystem enablement*
- *Integrating power-reducing methods, design techniques, and architectural enhancements*

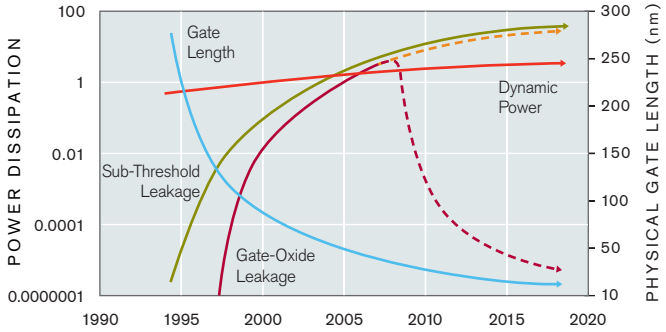
XILINX 28NM READINESS

2010 INNOVATIONS

For the foundation of its next-generation 28nm devices, Xilinx chose the high-κ metal gate (HKMG) high-performance, low-power (HPL) process pioneered by Taiwan Semiconductor Manufacturing Company (TSMC), which significantly minimizes static-power consumption. This process technology, jointly developed during the last five years, addresses the needs of customers who require high-quality performance and low power.

By collaborating with the best-in-class wafer fabrication teams at TSMC, Xilinx has introduced next-generation devices and platforms that improve time-to-market, increase return on investment, and minimize waste. TSMC's 28nm HPL process is a derivative of the foundry's high-performance HKMG technology and features low power, low leakage, and medium-high performance on a gate-last approach. It supports low-leakage applications for cell phones, smart notebooks, wireless communications, and portable consumer electronics.





Source: Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2002 Update. SEMATECH: Austin, TX, 2002.

Xilinx quality initiatives are making it possible to bring to market 28nm devices that comply with in-place quality standards and metrics. For the new 28nm devices, Xilinx introduced a structured technology readiness method based on lessons learned from previous technology generations. The latest methods include an enhanced development process that improves the stability of the technology. A new assessment methodology measures the degree of technology readiness and the risk involved in proceeding to development. The technology readiness method for 28nm, which delivers technological stability and device quality, includes:

- *A harmonized NPE/NPI process*
- *Design methodology improvements*
  - *Comprehensive performance verification with static timing analysis*
  - *Robust electrical verification though static circuit checks*
  - *Design-process interactions for better ESD protection*
  - *Design-for-manufacturability and reliability*
  - *Design-for-test*

CONT'D. >>

- *Product like test chips, incorporating key FPGA design blocks*
- *Software before silicon, which drives test development efficiency*
- *Enhanced verification and characterization, to prevent late discovery of critical issues*
- *Increased volume of corner materials, improving characterization test design*
- *Standard hardware, software, and IP verification process and rigorous focus on platform touch points for new architectures*
- *Capacity and manufacturing systems in place to support projected ramp-up*

28nm Design-for-Manufacturability (DFM) and Design-for-Reliability (DFR)

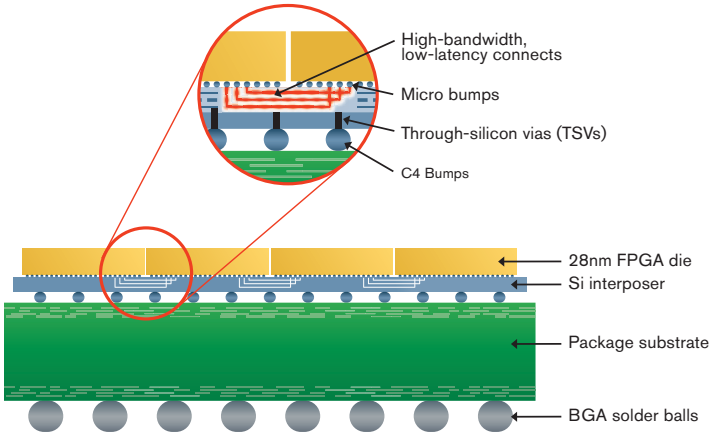
	28nm	40nm
TDDB	HSIMPlus → max (Vgs, Vgd) ≤ Vmax and area	N/A
NBTI	MO SRA simulation → EOL Performance	same
PBTI	MO SRA simulation → EOL Performance	N/A
HCI	MO SRA simulation ensures △Idsat < 5%	Ensured by DC LT and worst-case AC, DC factor (170)
NCI	MO SRA simulation ensures △Idsat < 5% with NCI stress	Limited case is allowed
EOL Performance	With both BTI and HCI effects considered	NBTI effect only
BEOL TDDB	More complete V-depend, space rule is checked by DRC	Simple V-depend, DR Si result, passed the worst case
BEOL EM	Width dependence EM rule in CAD tool	N/A

28nm DFM METHODOLOGIES		ADDRESSED ISSUE	VS. 40nm
DFM Rules	Redundant/rectangular via	Yield and EM reliability	Added rectangular via
	Gate and S/D contact placement	Yield and HK/MG gate resistance	Added HK/MG-specific rules
	Device secondary-effect-related rules	Device variation	Based on 28nm data
DFM Practices	Lithography process check (LPC)	Lithography hot spot	Using TSMC DDK
	FEOL/BEOL dummy fill	HK/MG and Cu CMP process uniformity	Added FEOL OPC dummy
	Virtual CMP (VCMP) simulation	CMP hot spot and metal thickness variation	New
	CD/overlay monitoring pattern	Process control, in-die variation	Added overlay pattern

FPGA INDUSTRY'S FIRST STACKED SILICON

2010
INNOVATIONS

The new Xilinx stacked silicon interconnect (SSI) technology enables an FPGA with more resources (logic, memory, serial transceivers, and processing elements) as well as breakthrough capacity and bandwidth performance. SSI technology also allows for multiple FPGA die to be combined, resulting in a 100x improvement in inter-die bandwidth per watt compared to conventional approaches.



SSI technology addresses the needs of applications such as next-generation wired communications, high-performance computing, and medical image processing. The highlights of this 2010 innovation include:

Leveraging existing 7 series die

- *SSI technology leverages reuse to allow characterized, tested, and qualified 7 series die to be combined in an array. This lowers risk since the silicon monoliths are not unique to each product.*

Silicon interposer technology

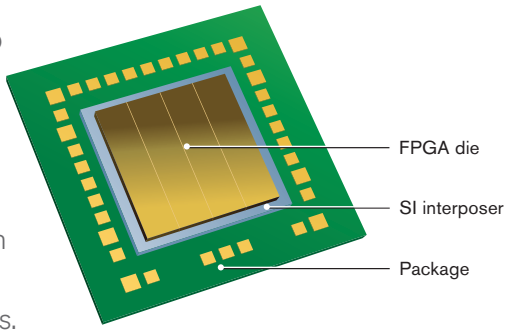
- *SSI technology is enabled by silicon interposer manufacturing on mature 65nm technology. Using three layers of copper and an aluminum redistribution layer (RDL), Xilinx is able to deliver a coefficient of thermal expansion (CTE)-compatible solution without added risk.*

World-class supply chain

- *Xilinx spent several years establishing a stable supply chain for this technology. TSMC and Amkor have been critical partners, contributing to the successful delivery of this milestone FPGA advancement. These manufacturers are recognized for not only technology, but also robust quality and product reliability that customers have come to expect.*

By combining through-silicon via (TSV) and micro bump technologies with its innovative ASMBL™ architecture, Xilinx is building a new class of FPGAs that delivers the capacity, performance, capabilities, and power characteristics required for next-generation systems and products.

CONT'D. >>



The figure here shows the top view of the die stack-up with four FPGA die slices, silicon interposer, and package substrate. Xilinx SSI technology combines enhanced FPGA die slices and a passive silicon interposer to create a die stack with tens of thousands of die-to-die connections. The results include ultra high inter die interconnect bandwidth with far lower power consumption and one-fifth the latency of standard I/Os. The silicon interposer acts as a micro-circuit board in silicon, on which up to four die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues that can result from stacking multiple FPGA die on top of each other by using well-understood, compatible technologies. Compared with organic or ceramic substrates, silicon interposers offer far finer interconnect geometries (approximately 20x denser wire pitch) to provide a device-scale interconnect hierarchy that enables more than 10,000 die-to-die connections.

Since 2009, Xilinx has been working with its world-class partners to develop the SSI technology. Various test vehicles have been taped out and packaged over this period to study the reliability, manufacturability, and yield of the micro-bumps and TSVs. We have also performed extensive chip-package modeling and correlation with test vehicles in order to shorten the learning cycle and provide early assessment of potential risks. All manufacturing issues have been fully addressed and risk mitigations have been put in place using failure mode efficiency analysis (FMEA) and control plans. This technology will be released to production upon the completion of qualification, verification, and characterization based on Xilinx NPE/NPI requirements proven on Virtex®-5 and Virtex-6 FPGAs.

As the only FPGA manufacturer to use SSI technology to create super-high-capacity FPGAs with unmatched die-to-die bandwidth, Xilinx is breaking important new ground. SSI technology will allow Xilinx to deliver the highest logic density, bandwidth, and on-chip resources with the fastest ramp to volume production of any previous process node. Customers will be able to leverage streamlined design processes compared with the alternative multiple-FPGA designs.

TECHNOLOGY ELEMENT	DETAILS
TSMC	28nm HPL process node
	Hi-k dielectric / metal gate
	10 copper layers
	1 aluminum layer RDL
Silicon Interposer	TSMC 65nm process node
	Copper TSV
	3 copper layers
	1 aluminum layer RDL
Flip-Chip Package	Plated eutectic (63% Sn / 37% Pb)
	TSMC package bumping
	Amkor die bumping

2010
INNOVATIONS

TEST CHIPS

A Product Process Learning Vehicle (PPLV) for 28nm

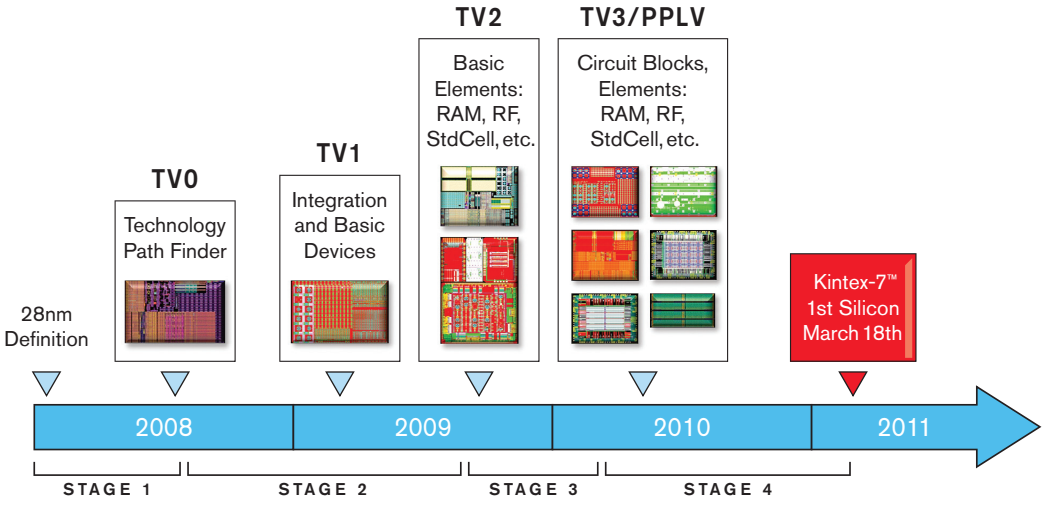
Xilinx began using test chips more than 10 years ago to streamline development for new process technologies. Now, many generations later, the role and capability of the test chip have expanded significantly. Today's test chips incorporate key design blocks — RAM, SerDes, die stacking, monitor vehicles, and benchmark circuits — to help uncover and overcome process challenges early in development.

In general, test chips allow:

- *Detection of design marginalities and feedback to product design*
- *Validation of power, performance, and reliability*
- *Key design, process, and layout interdependencies*
- *Pre-qualification learning and fault isolation ahead of product silicon*

During process definitions with Taiwan Semiconductor Manufacturing Company (TSMC), Xilinx employed test chips to accelerate and improve the development for its selected 28nm process. Product process learning vehicles (PPLVs) offered many benefits including adding cycles of learning that improved quality earlier in the life cycle. Test chips also regularly speed time to market for FPGA development since they provide detailed process technology look-ahead in the areas of yield enhancement (better understanding of defects), performance predictability, and reliability.

More than two years of technology development using test vehicles



CONT'D. >>

Xilinx's unique PPLV approach contributed to the optimization of process parameters while also providing better circuit-modeling enhancement for the 7 series designs. To further understand the challenges of the 28nm generation, test chips also enabled learning cycles relating to:

- *Package-level LC VCO (return loss characterization)*
- *Further characterization and reliability assessment on RAM test chips and stacked die*
- *Corner silicon evaluation and characterization*
- *Benchmark monitors from new silicon*

Key Benefits of Xilinx PPLV

- *Package- and board-level characterization for functionality and leakage of SerDes elements (exercise chip similar to product and identify any potential design marginalities)*
- *Electro static discharge (ESD) charge device model (CDM) solution validation on GT SerDes and VBRAM power pin*
- *Wafer-level characterization from macros and correlation to package-level data and radio frequency (RF) test keys*
- *Parametric yield, hard/soft-bit fail learning, fault isolation, and failure analysis (FA)*
- *Characterization over device corners*
- *Early pre-qualification data, fault isolation, and FA results based on reliability tests such as high temperature operating life (HTOL), temp cycle (TC), high accelerated stress test (HAST), and biased temperature instability (BTI)*
- *Early single-event upset (SEU) learning and validation*