XILINX

ALL PROGRAMMABLE™

All Programmable: from Silicon to System

Ivo Bolsens,
Senior Vice President & CTO

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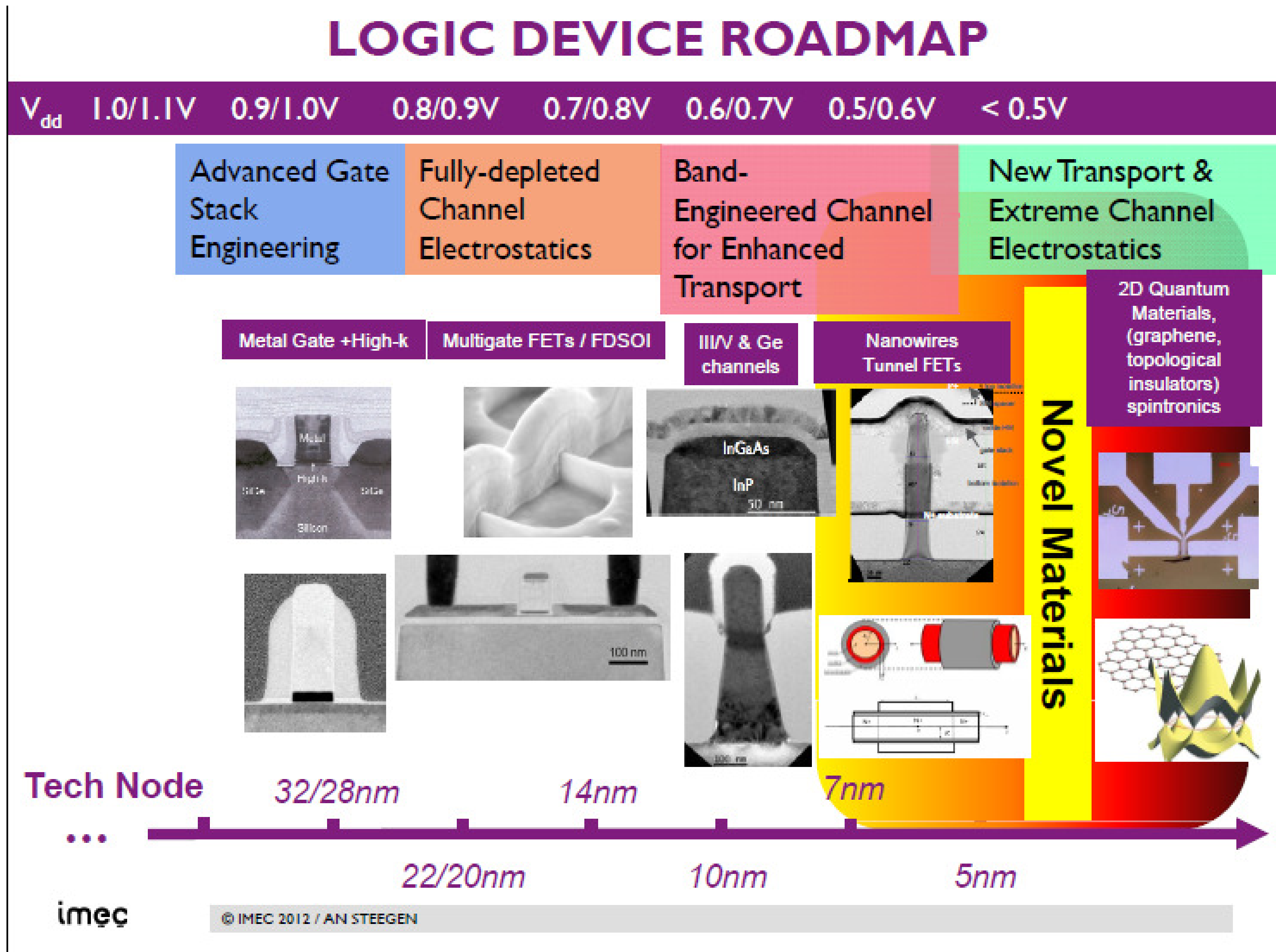
Moore's Law: The Technology Pipeline



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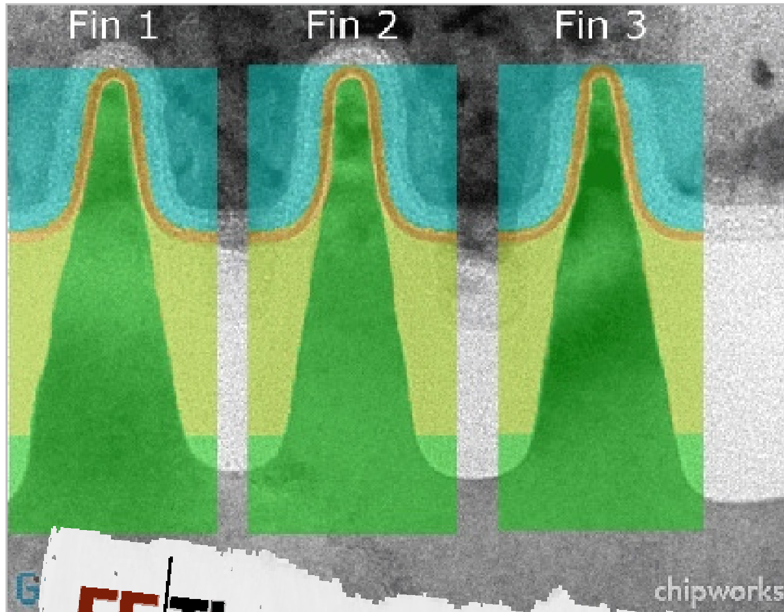
Industry Debates Variability



EE Times

IMEC looks at variability beyond 10 nm

Anne-Françoise PELE
6/1/2012 5:10 PM EDT

PARIS – CMOS technology scaling will go on for the foreseeable future but, as we enter the 10nm node, process complexity reduction and variability control will become crucial and drive technology decisions, said An Steegen, senior vice president process technology at Imec, at the annual IMEC Technology Forum last week at the Square meeting center in Brussels, Belgium.

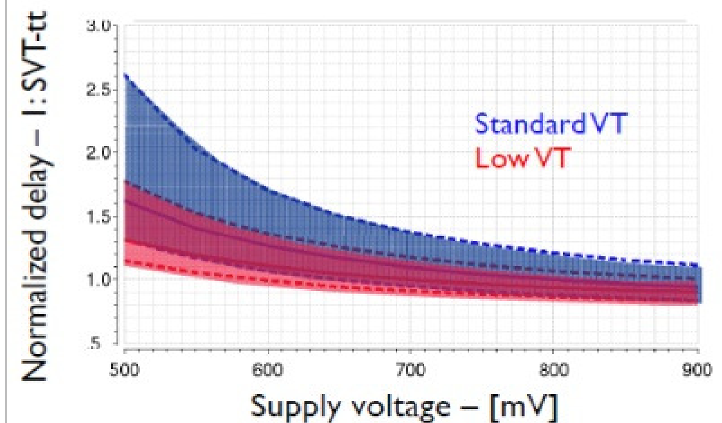
EE Times

Intel FinFETs vary, may need SOI for shrink, says GSS

Peter Clarke
6/6/2012 7:01 AM EDT

LONDON – Intel's 22-nm FinFETs show physical variability according to cross-sectional photographs from engineering consultancy Chipworks Inc. (Ottawa, Ontario) and EDA company Gold Standard Simulations Ltd. (GSS) has attempted to model electrical characteristics of various examples.

One conclusion drawn by Professor Asen Asenov, CEO of GSS (Glasgow, Scotland), is that Intel may need to turn to silicon-on-insulator wafers to scale its FinFETs below 22-nm. This may also have implications for foundries which are yet to introduce FinFET technology into their chip manufacturing processes.



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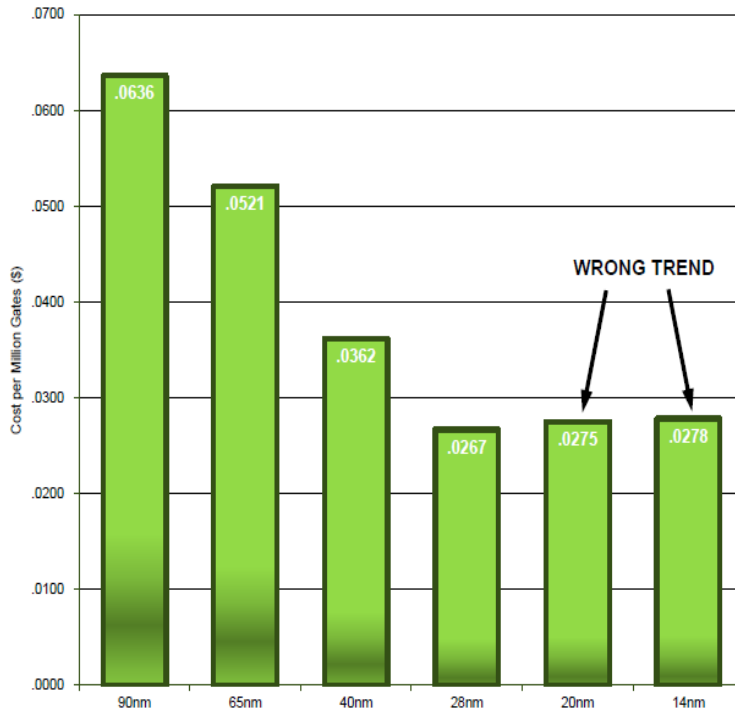
Industry Debates on Cost



ARM 20nm Processors Expected to Arrive Next Year

Douglas Perry
6/5/2012 6:00 PM EDT

The chip manufacturing race is heating up and Intel could be ... pressure down the road.

Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless

Joel Hruska
March 23, 2012 at 12:13 pm

One of the unspoken rules of customer-foundry relations is that you virtually never see the former speak poorly of the latter. Only when things have seriously hit the fan do partners like AMD or Nvidia

TSMC raises capex to record $8.5 billion, pulls in 20-nm

Peter Clarke
4/26/2012 12:23 PM EDT

LONDON – Taiwan Semiconductor Manufacturing Co. Ltd. has raised its planned capital expenditure for 2012 to between $8 billion and $8.5 billion. The move accompanied the announcement of first quarter financial results and strong second quarter outlook by the foundry.

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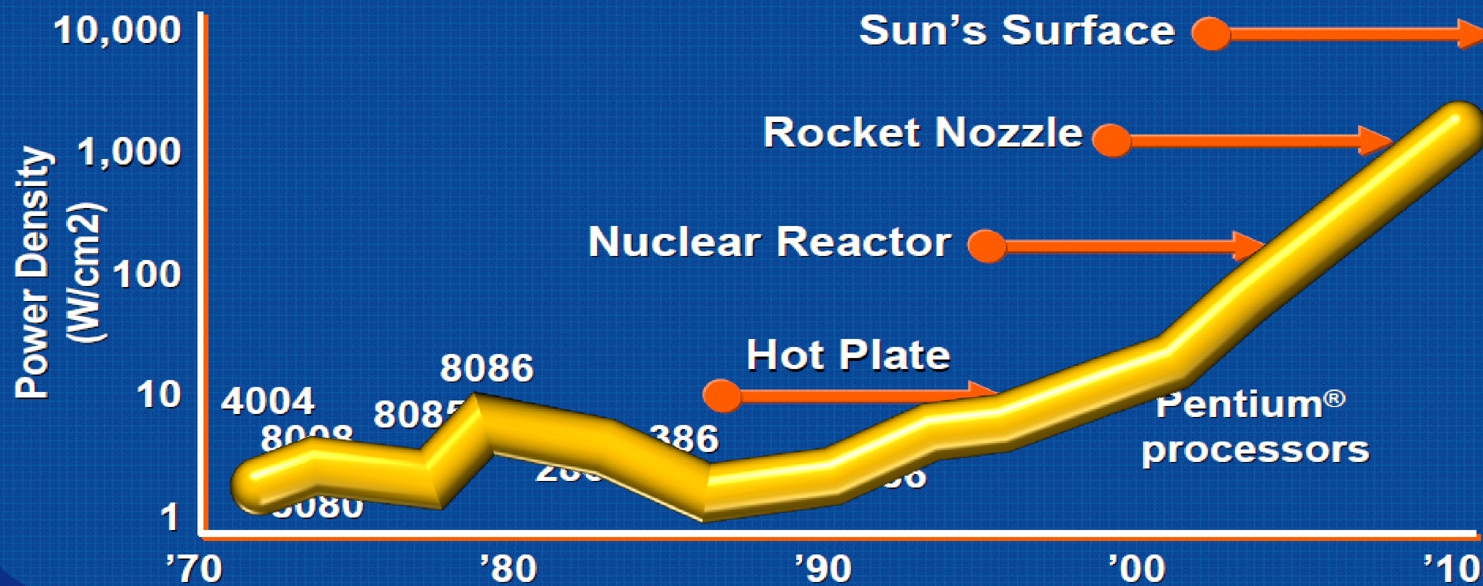
Nothing New: Power Challenge



Multi-Core

Source: Intel

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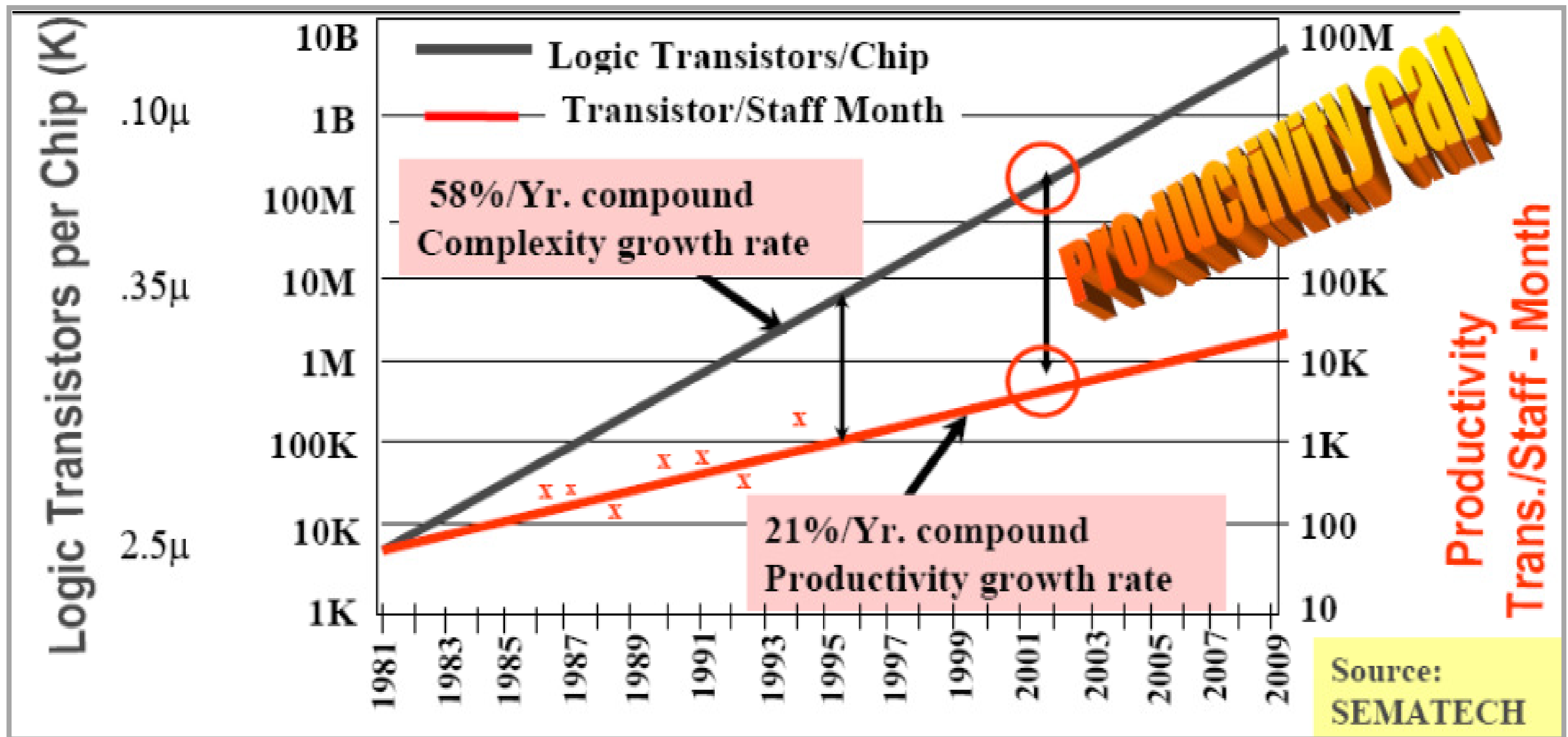
Nothing New: Productivity Gap



ESL Design Flow
IP Re-Use

Source: SEMATECH

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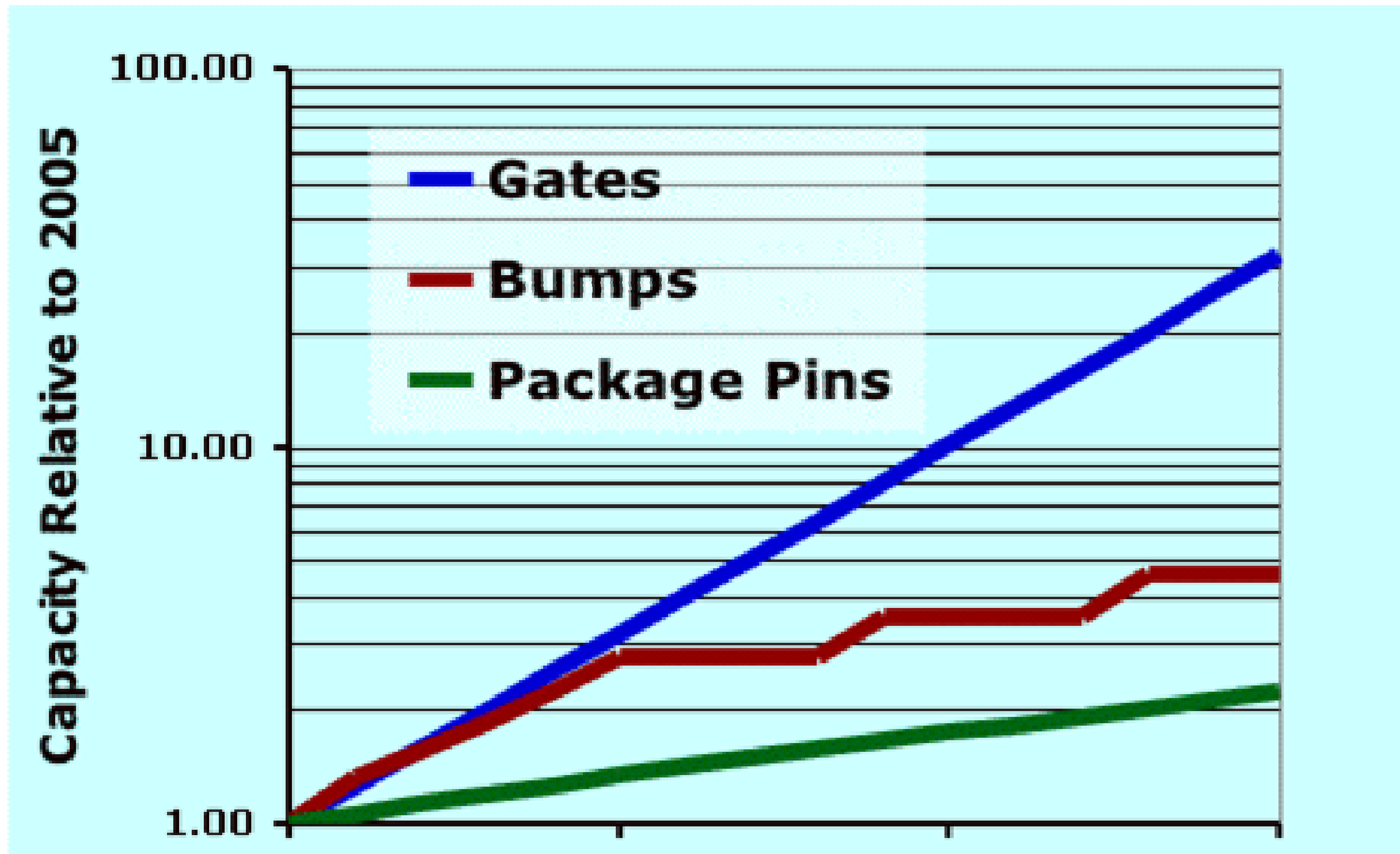
Nothing New: I/O Bandwidth Gap



Multi-Gigabit SerDes

Source: Xilinx, Inc.

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"Doubt is not an agreeable condition, but certainty is absurd."

François-Marie Arouet de Voltaire, French Philosopher

Photo Source: Wikipedia

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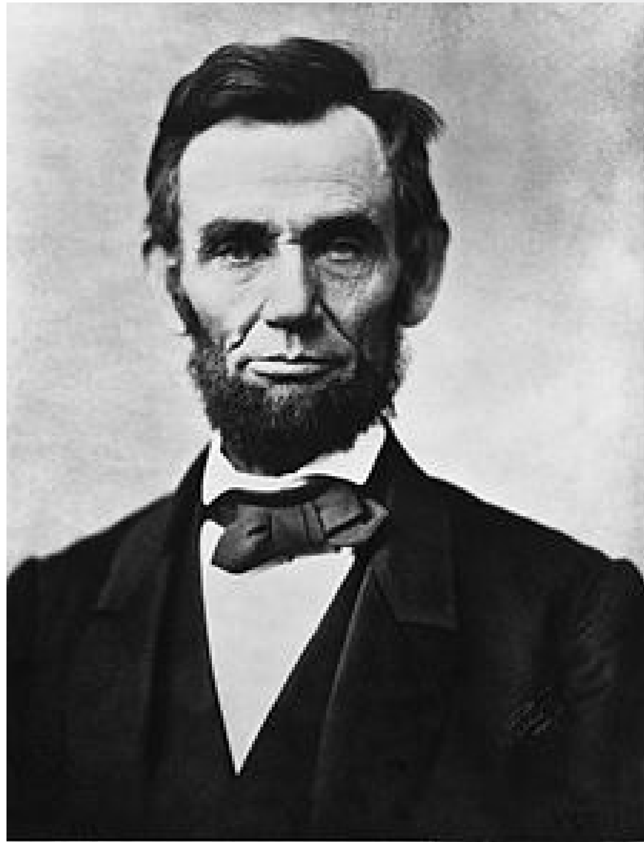

"Don't believe everything you read on the Internet."

Abraham Lincoln,
U.S. President

Photo Source: Wikipedia

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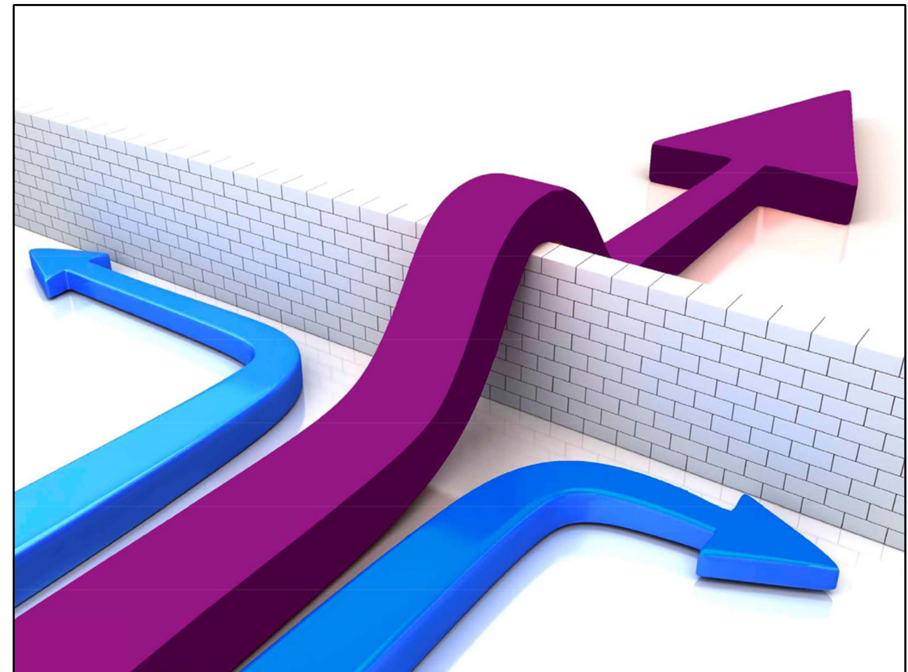
Extending and Leveraging Moore's Law

- **Add Value : Programmable System Integration**
  - Programmability
  - 3D Integration
- **Collaborate**
  - Supply Chain
    - Wider – more Complexity
    - Deeper – earlier Engagement
  - From System to Silicon



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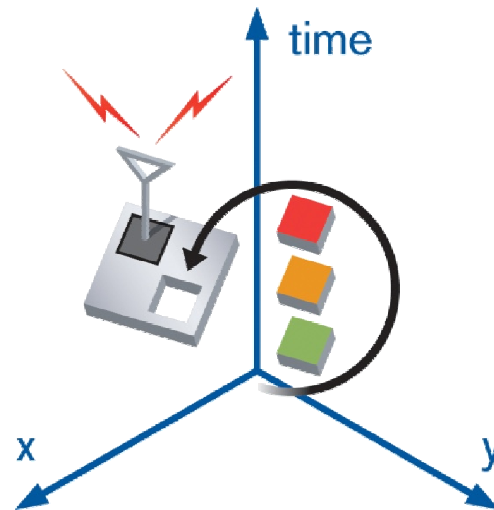
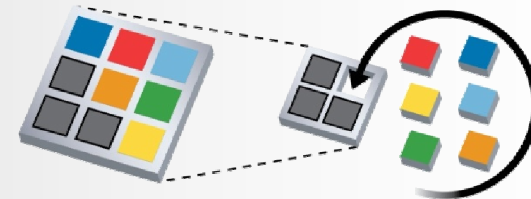
Value of Programmability: Configurability

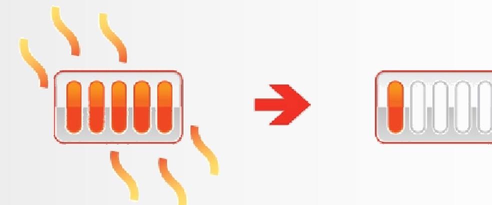


Partial Reconfiguration

– Time-multiplexing hardware



Lower Power



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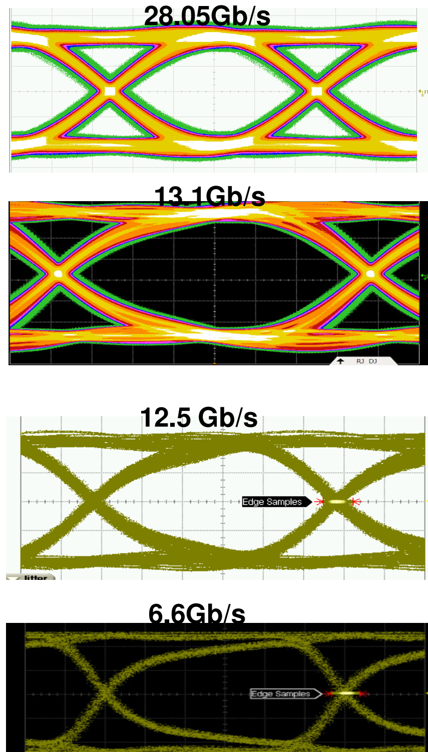
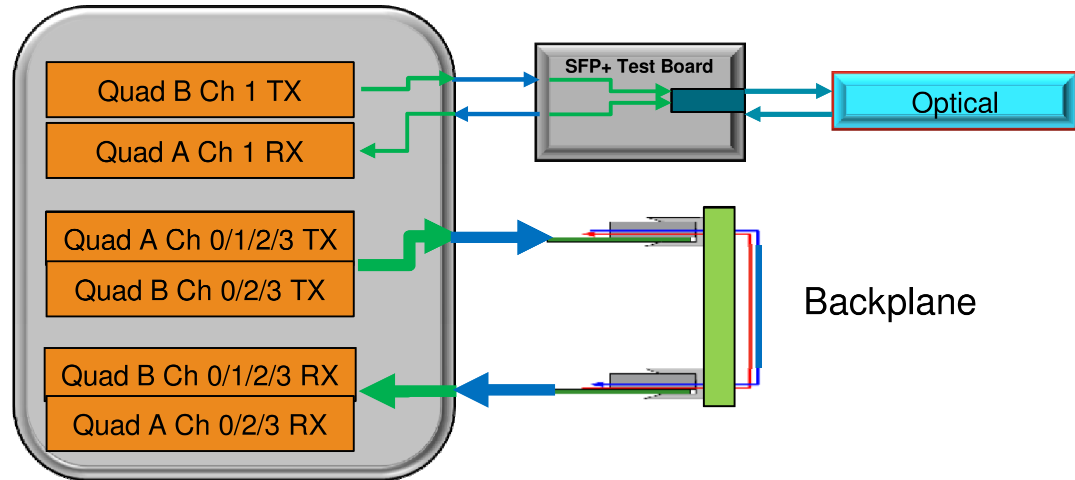
Value of Programmability: I/O





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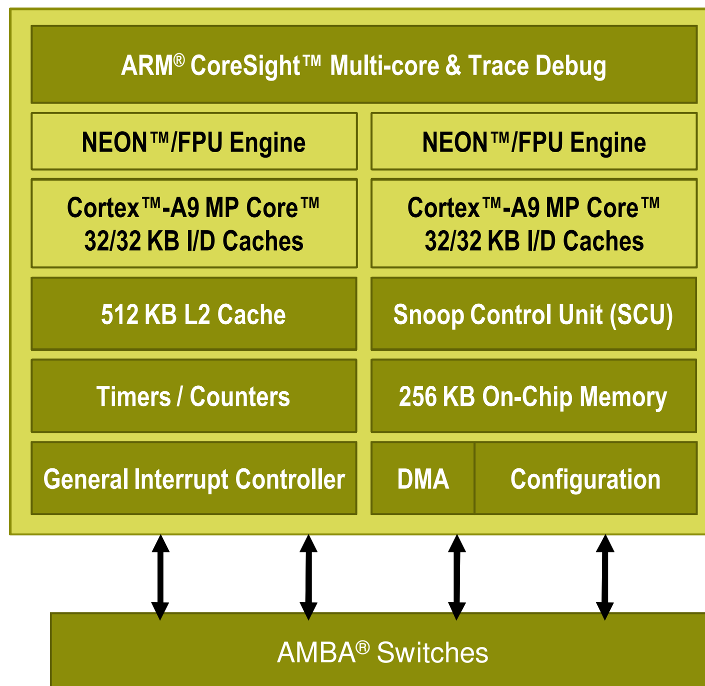
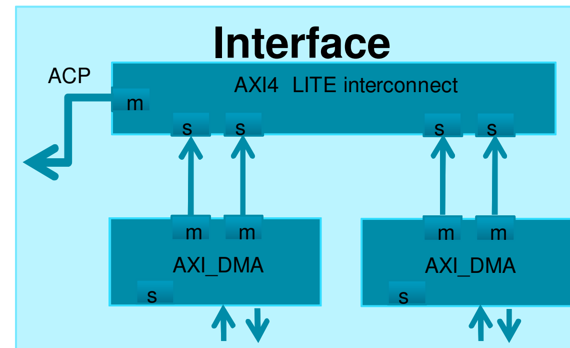
Value of Programmability: GOPS/Watt





From 100 Watt to 2 Watt

10x Performance Acceleration

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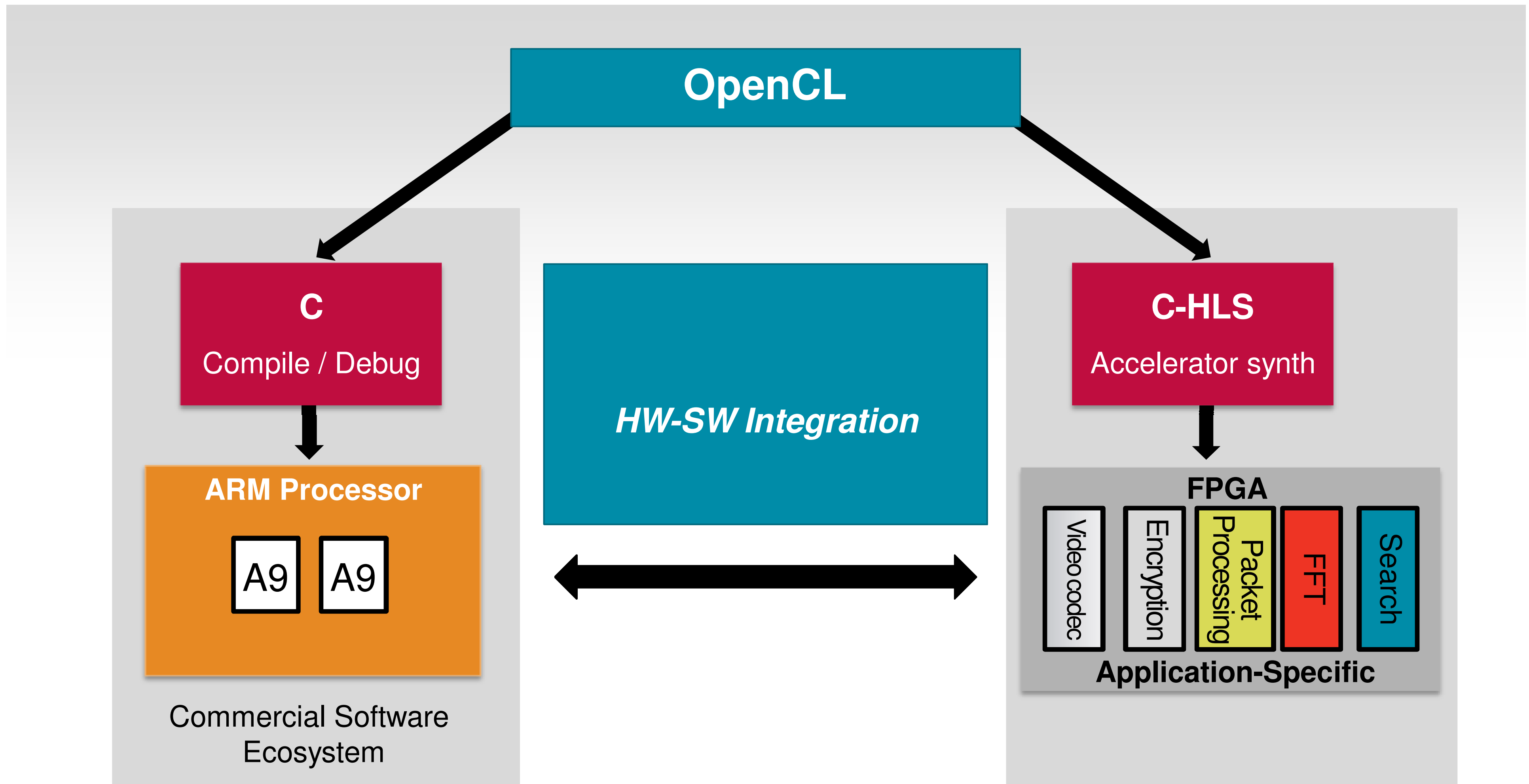
Future Challenge: HW + SW co-design



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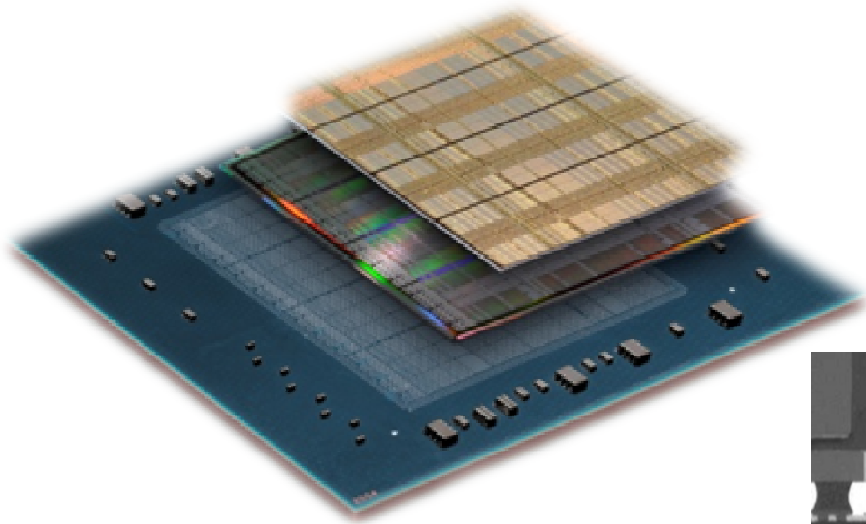
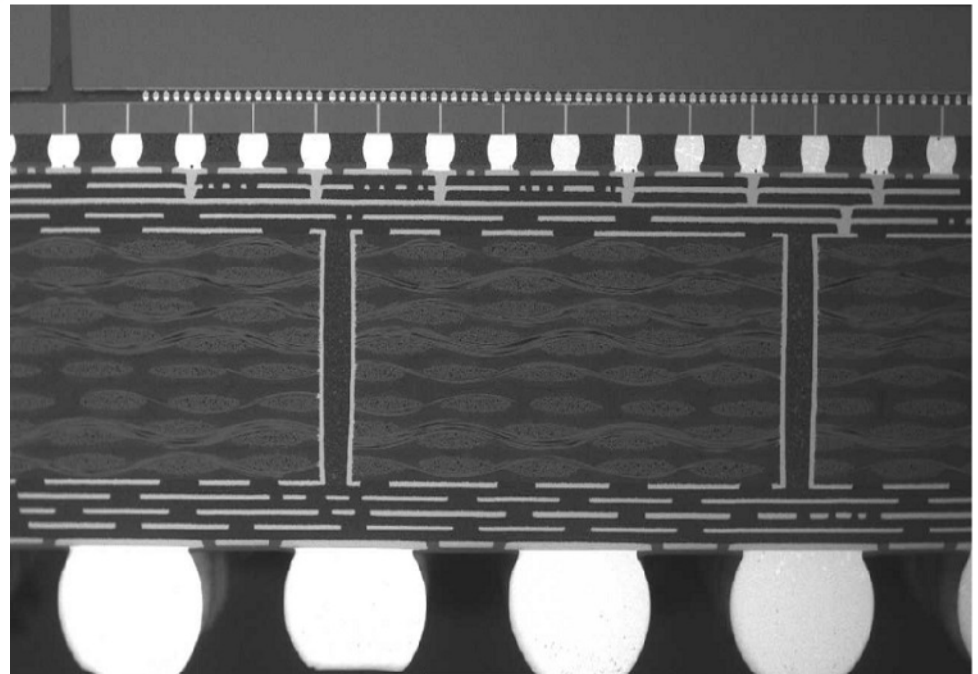
3D Integration: Add Value





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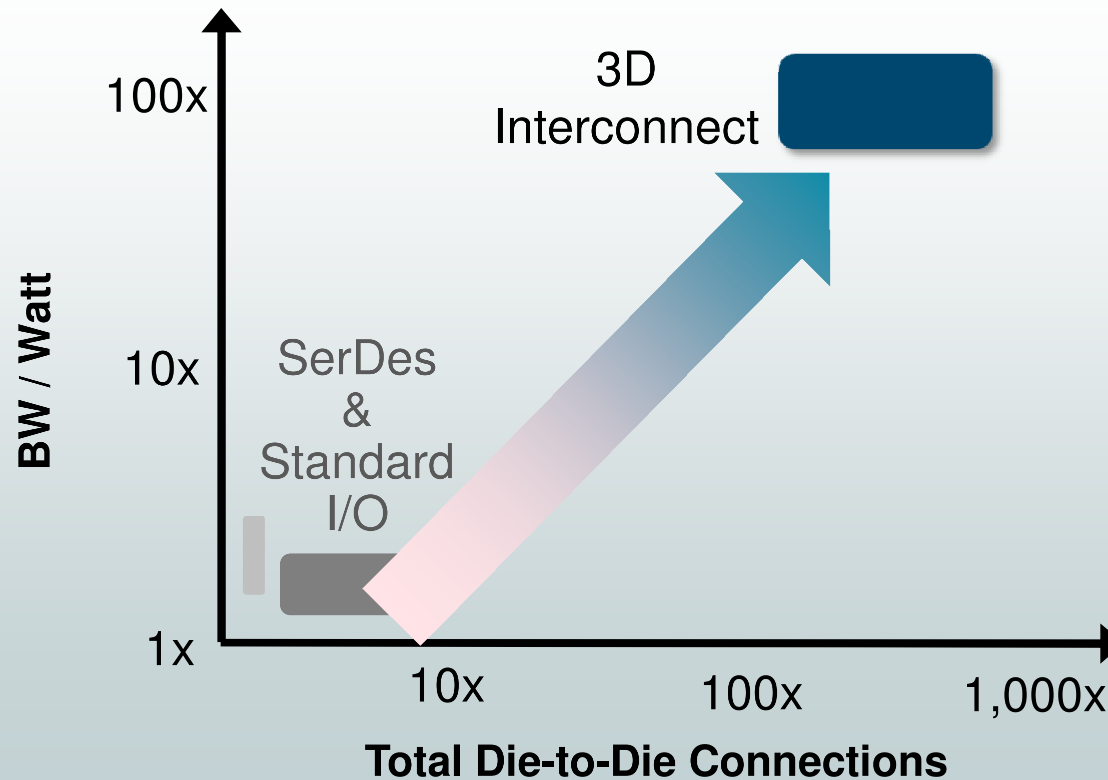
Value of 3D Integration: Bandwidth/Watt



100x bandwidth/watt advantage over conventional methods

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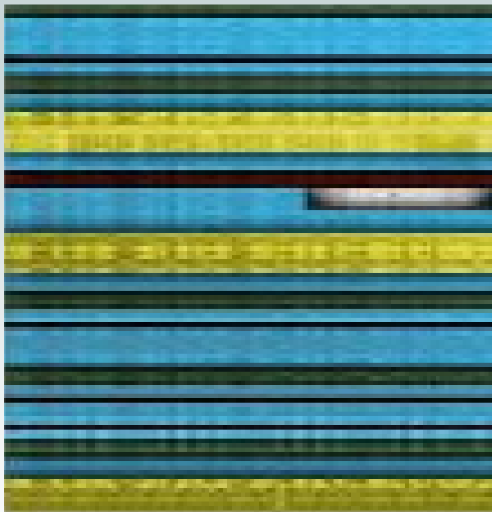
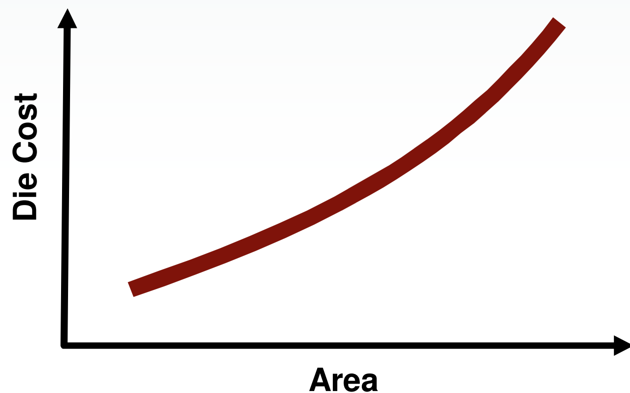
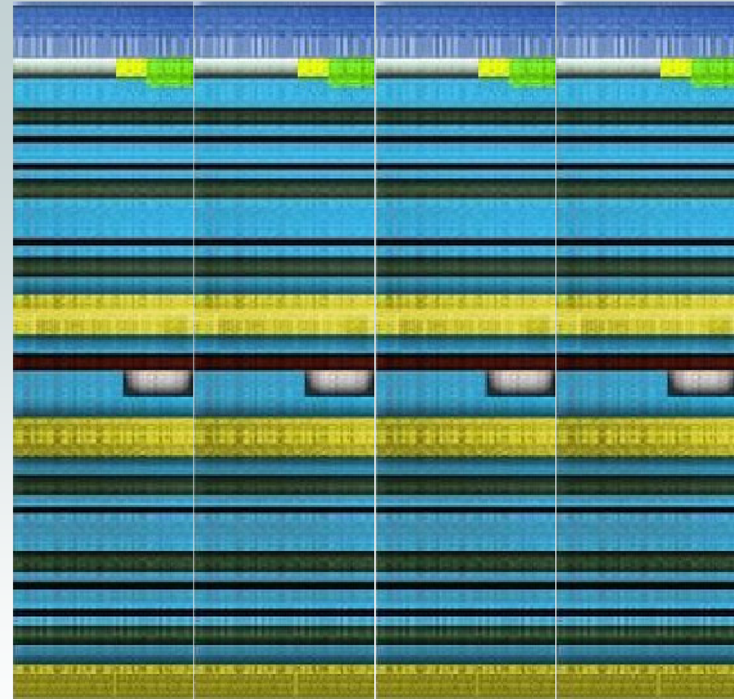
Value of 3D Integration: Cost/Gate

Big Single Monolithic Die



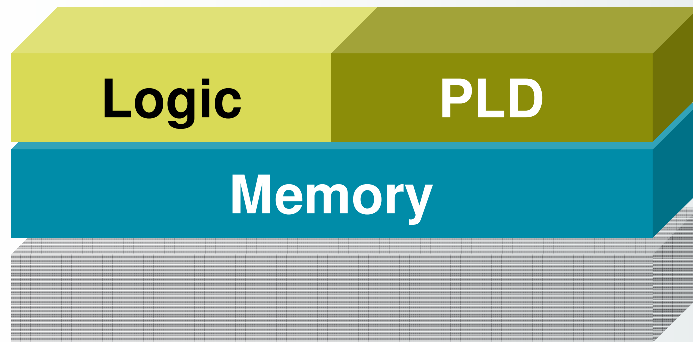


Multiple Small Die Slices

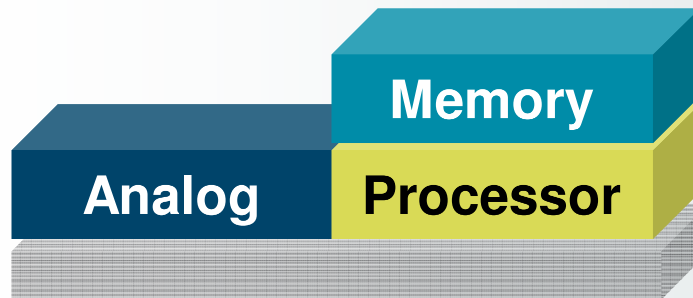


- Greater capacity, faster yield ramp

Value of 3D Integration: Heterogeneous ICs



Mixed functions



Mixed processes

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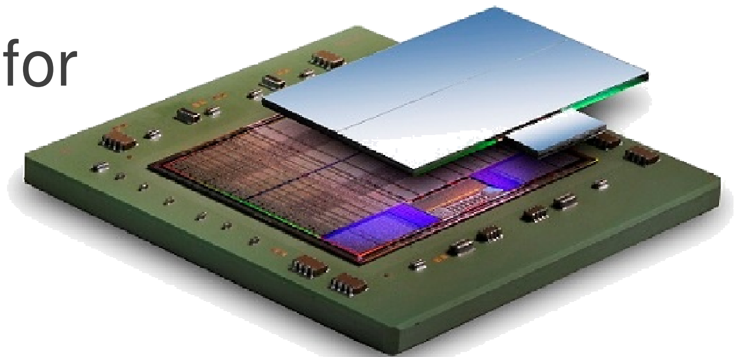
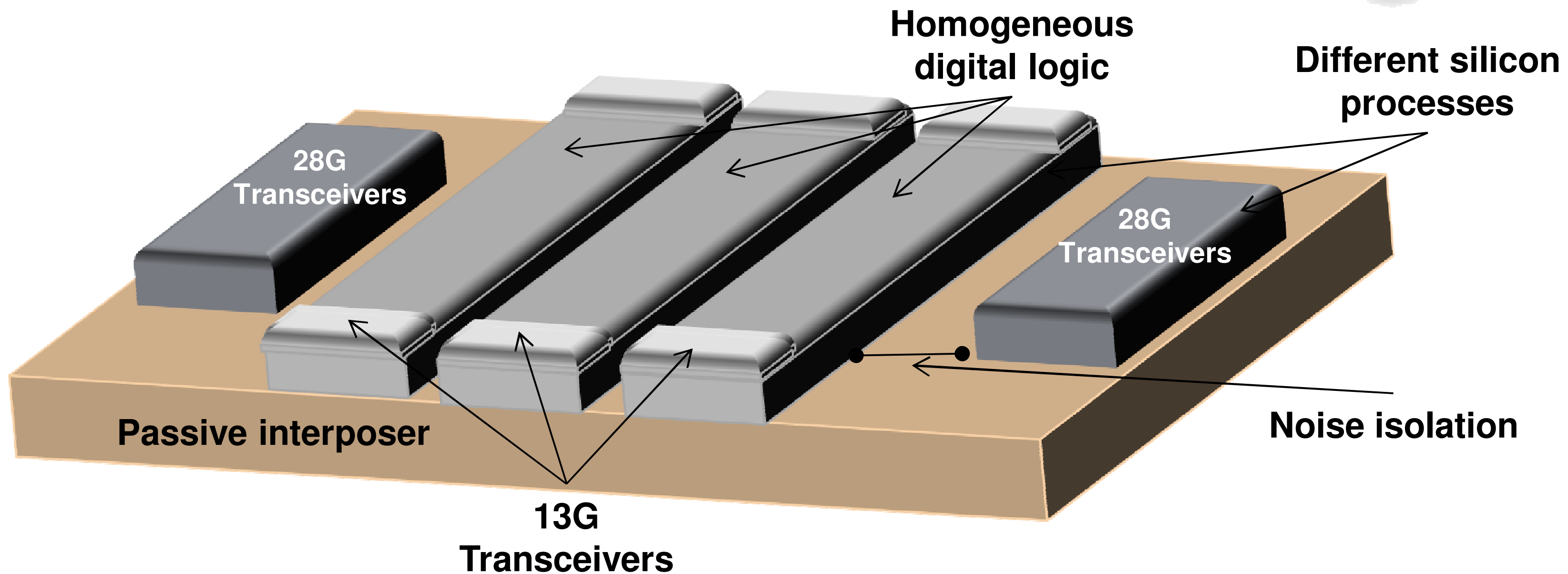
Value of 3D Integration: Heterogeneous ICs

- Highest bandwidth FPGA with 2.78 Tb/s serial connectivity
- Electrically-isolated 28G transceivers for optimal signal integrity





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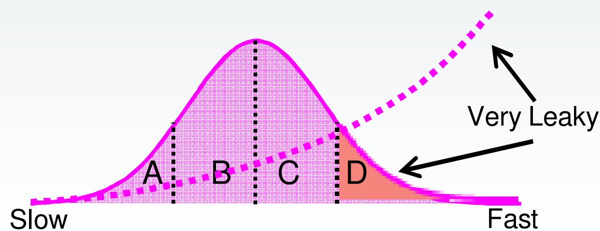
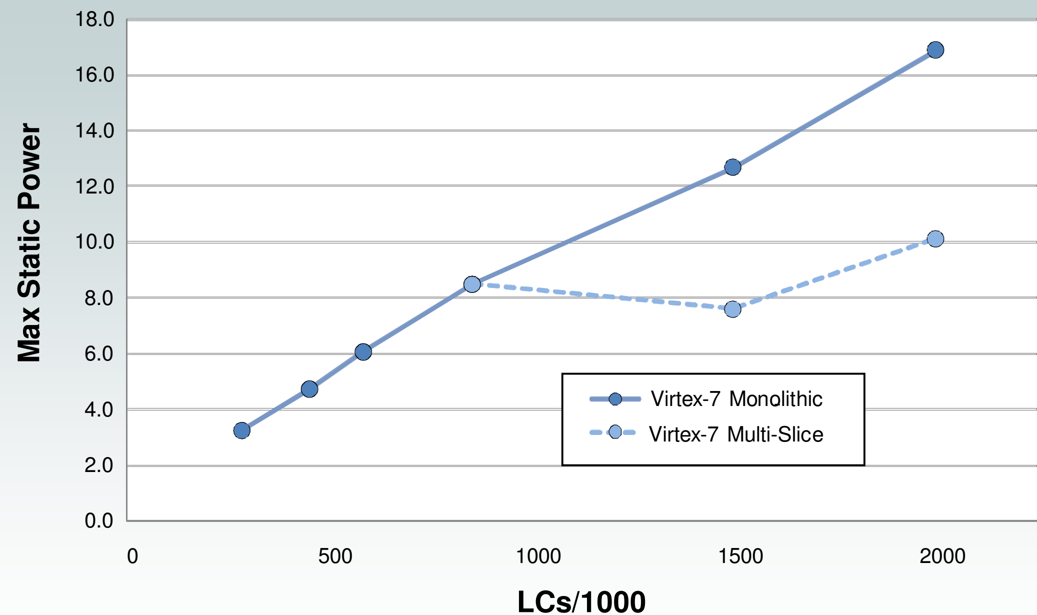
Value of 3D Integration: Lower Power

Silicon Interposer with 28nm FPGA Slices



7 Series Static Power vs. Logic Cells at Tj=85C and Max Process



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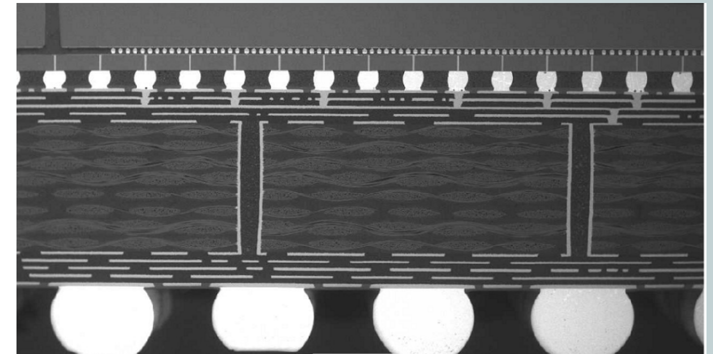
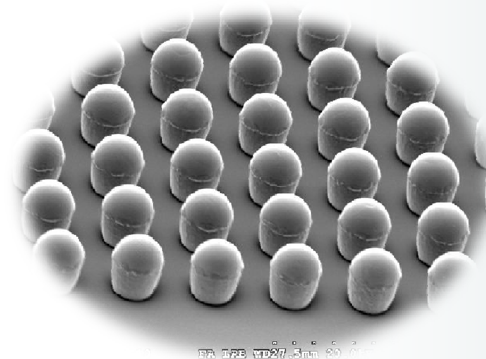
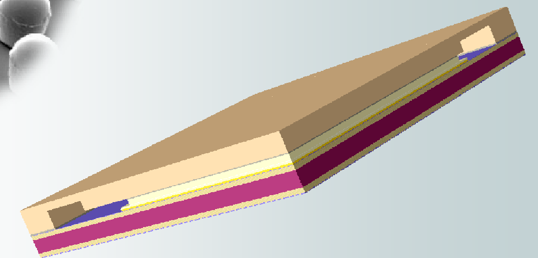
3D Integration: Challenges Ahead



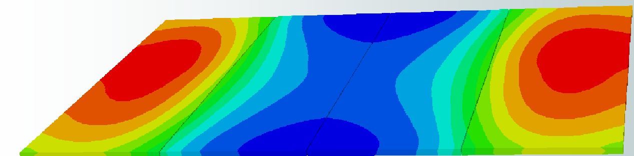
- **Improve Cost**
  - Wafer backside processing is complicated
  - "Device quality" wafers used for interposers
  - KGD methodologies still emerging



- **Scalability**
  - Micro-bump scaling is limited
  - Super-sized interposers.
  - Improve TSV aspect ratio



- **Design Support**
  - Multi-die analysis without Multi-mode Multi-corner explosion
  - Thermal modeling based on vertical hotspots



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3D Integration: Industry Call-to-Action

Design Enablement

- Models
- 3D Process Development Kit

Manufacturing Standards

- DFM rules for TSV, μ-bump
- Materials TSV, μ-bump
- Thermal budget

Test

- Test HW
- Known-good-die method
- μ-bump probing
- Burn-in bare die

Interoperability of Silicon

- Thin wafer handling
- Shipping methods
- Chip-to-chip interfaces

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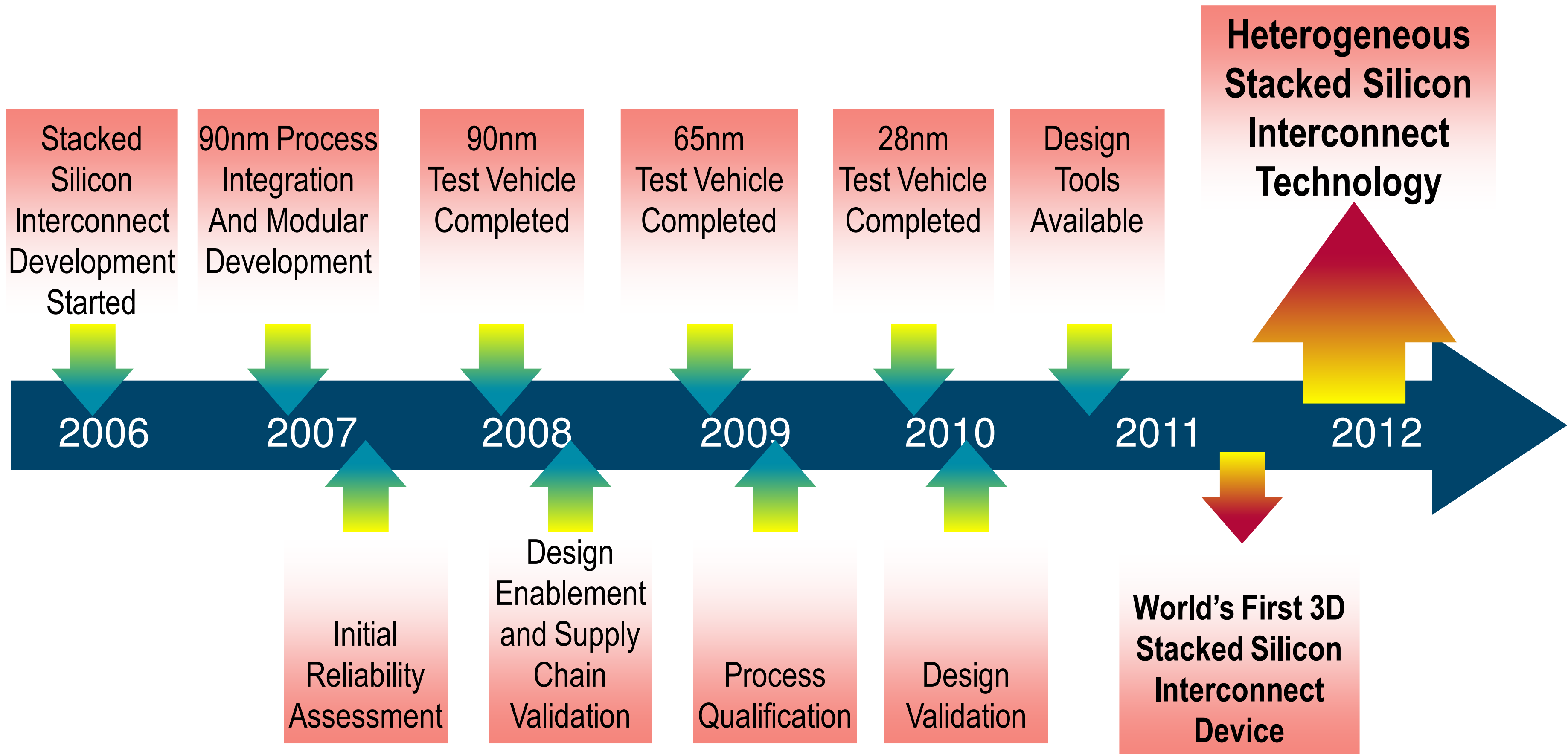
Supply Chain Collaboration: Early Engagement



3D Integration

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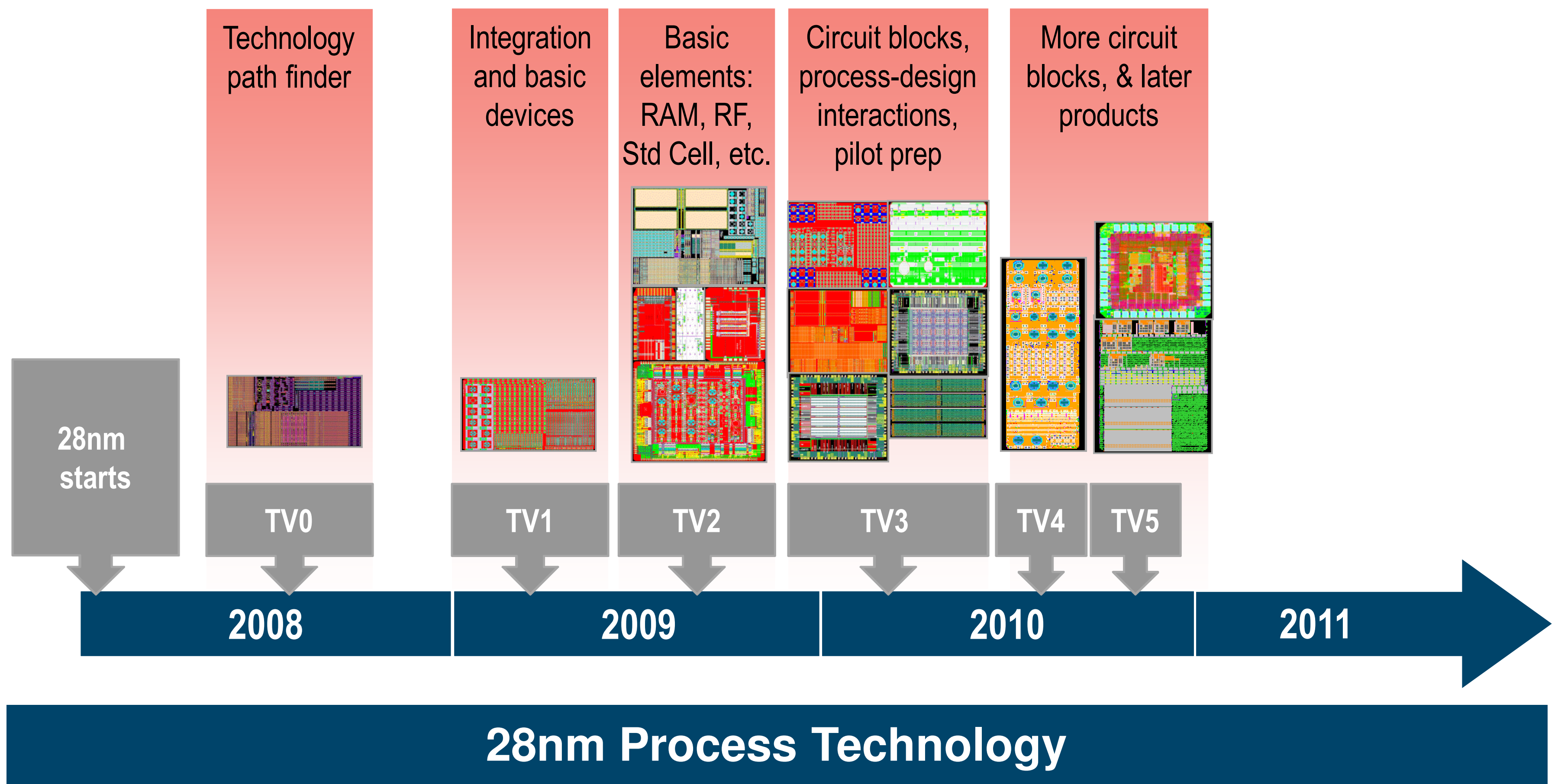
Supply Chain Collaboration: Early Engagement



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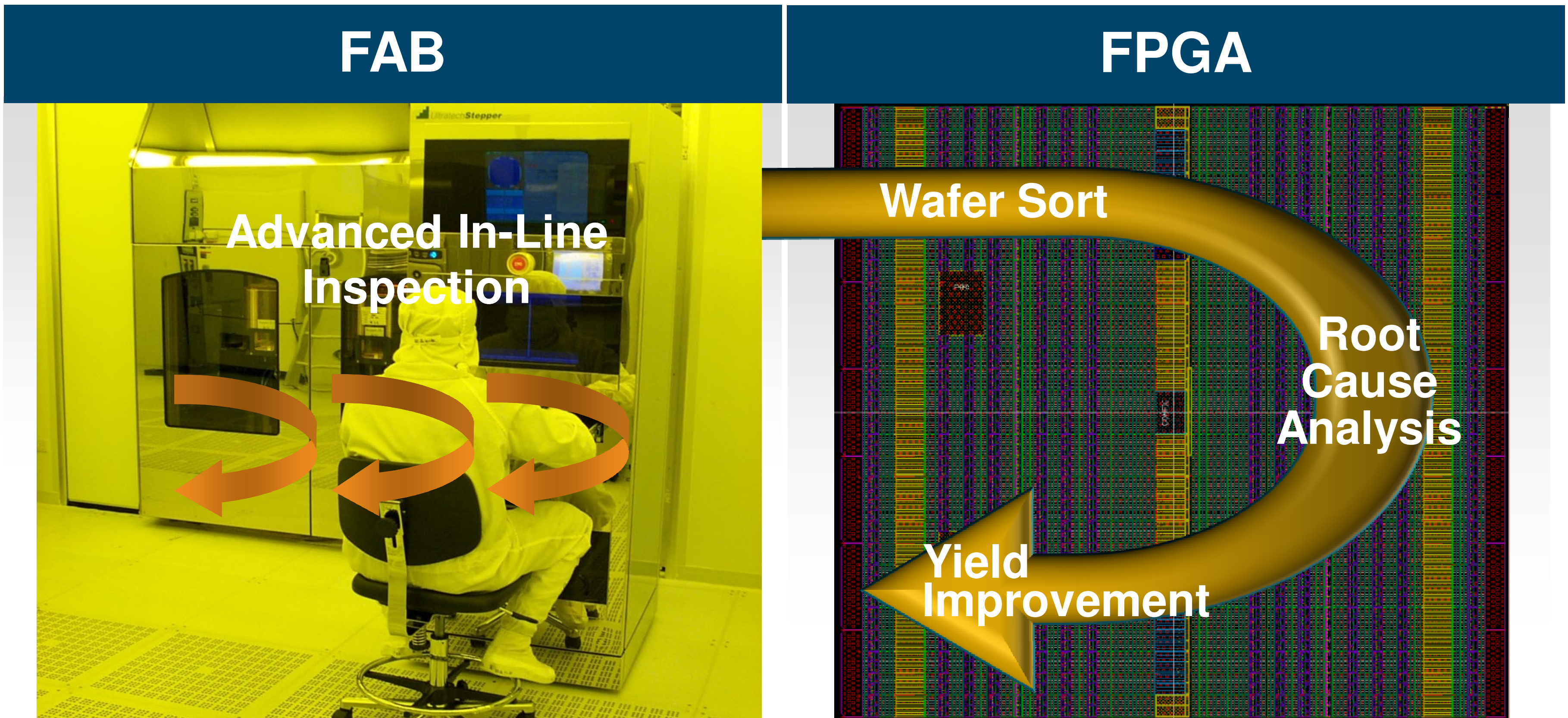
Supply Chain Collaboration: Product Ramp Up



- Continuous, early feedback loop for initial ramping
- Enables accelerated learning – days vs. months

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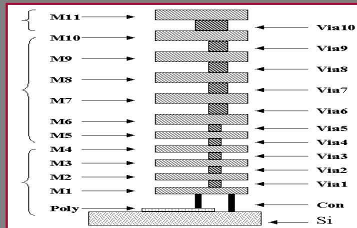
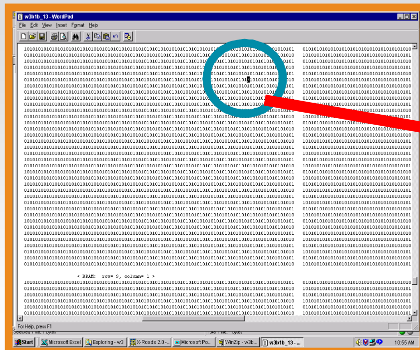
Supply Chain Collaboration: Mutual Benefit

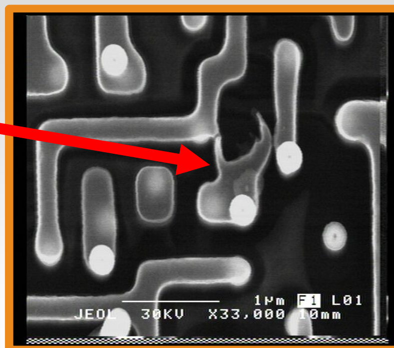
- FPGA architecture drives yield & quality improvements



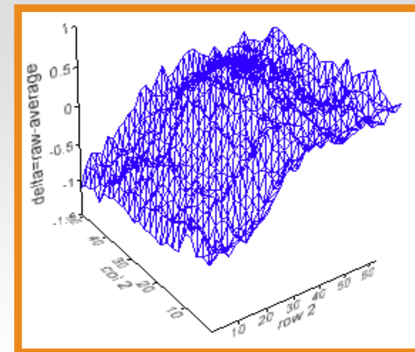
The FPGA is a powerful yield learning vehicle with multiple layers of programmable features

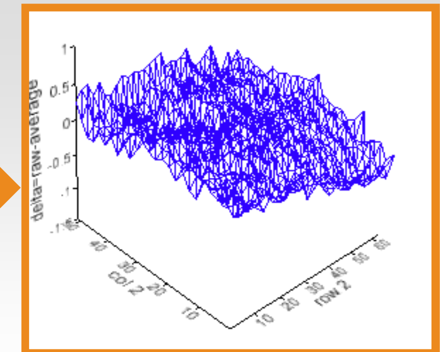
Defect Reduction:
quick to detect defects
If you can't find it, you can't fix it





Process Control:
powerful to measure variations
If you can't measure it, you can't improve it





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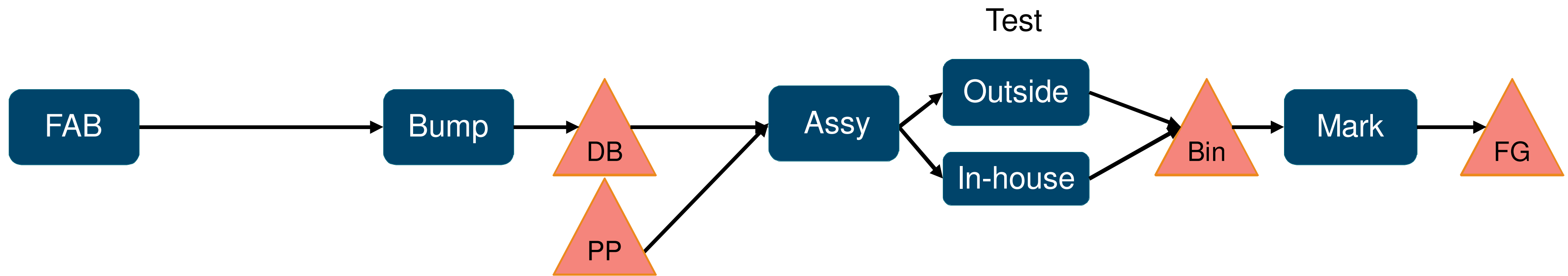
Supply Chain 1998 - 2010



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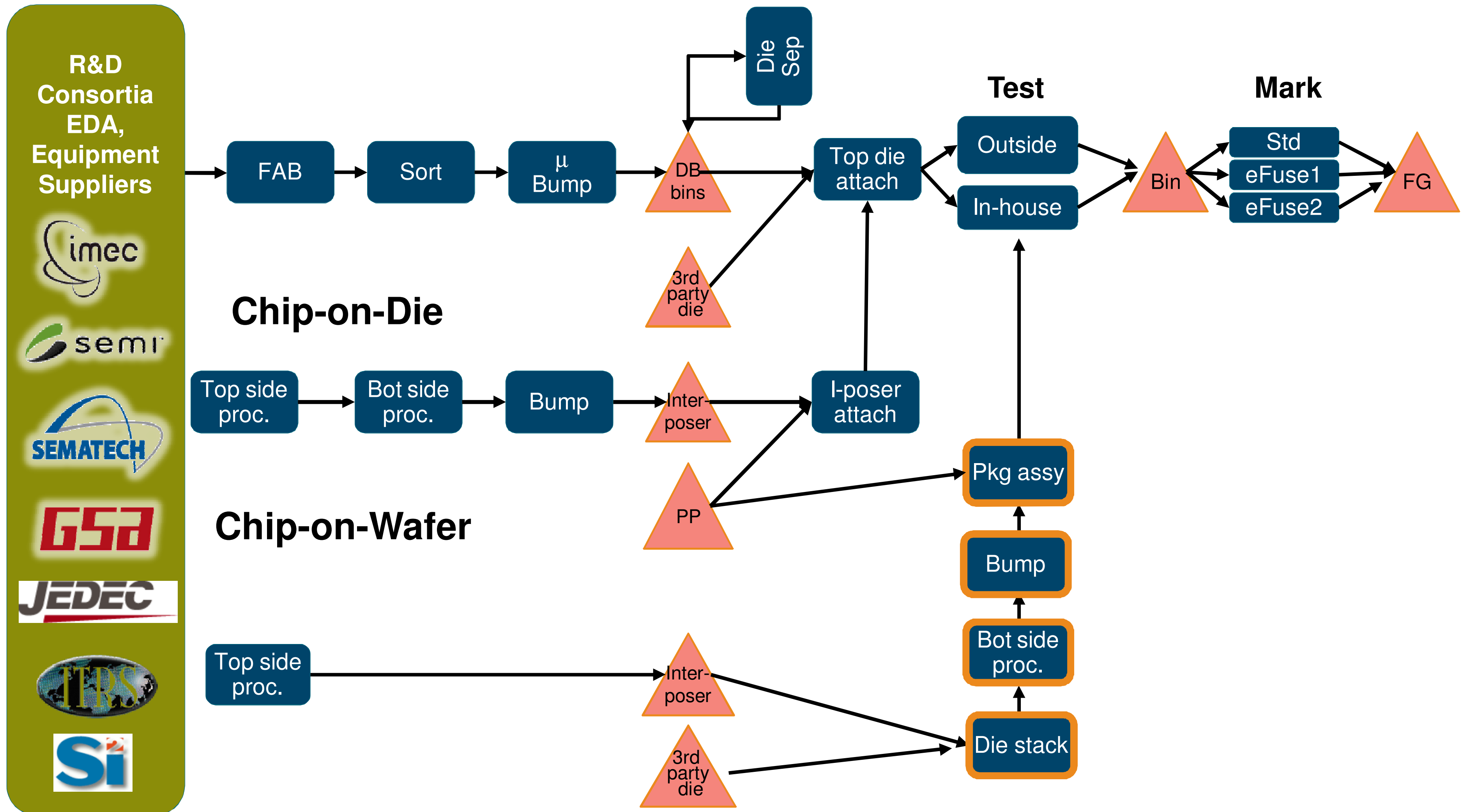
Today's Supply Chain



Wider and Deeper

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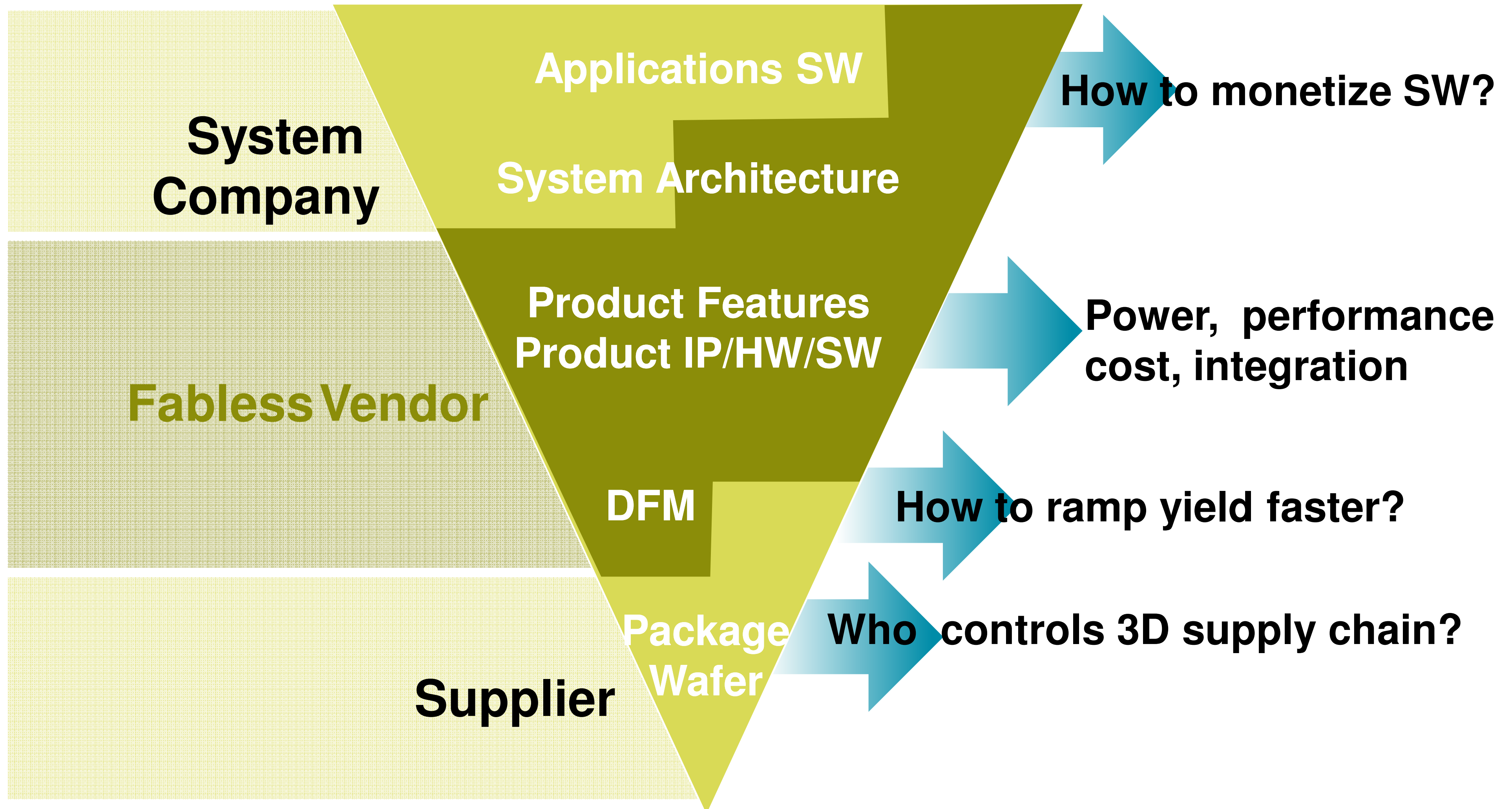
From Silicon to System



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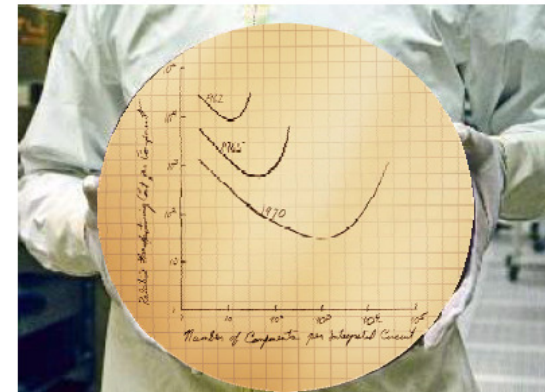
Conclusions

- Moore’s Law:
  - From mostly cost reduction to more value-based innovation
- System figure of merit defines value
- Xilinx programmable system integration
  - Programmability
  - 3D integration
- Supply chain partnerships to enable
  - Efficiency
  - Standardization
  - Innovation



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What Xilinx Makes Possible:

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ALL **Programmable Electronic Systems**

ALL **Programmable Technologies**

ALL **Programmable Devices**

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