2.5D ICs: Just a Stepping Stone or a Long Term Alternative to 3D?

Ivo Bolsens, CTO Xilinx

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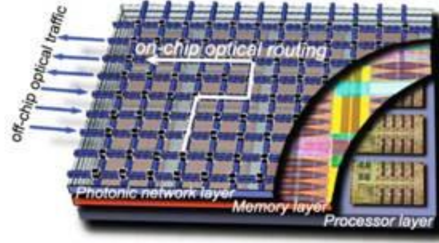
The First Wave of 3D ICs

ElectronicsWeekly.com

IBM Demonstrates 3D Chip Technology in Micron Memory Cube

Richard Wilson
Friday 02 December 2011 00:01

IBM has announced that Micron will begin production of a memory device built using its commercial CMOS manufacturing technology to employ through-silicon vias (TSVs).



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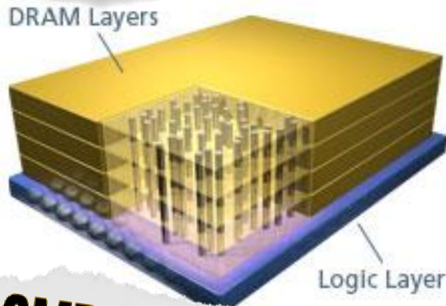
THE DISRUPTIVE SEMICONDUCTOR TECHNOLOGIES WEBSITE
FROM CONCEPT TO DEVICES
TECHNOLOGIES, FINANCE, BUSINESS, MARKETS...

> ADVANCED PACKAGING: 3D IC, WLP & TSV

Feb 18th, 2011

Micron reveals "Hyper Memory Cube" 3DIC Technology

A few weeks ago Mark Durcan, COO of Micron, at the IEEE ISS meeting in Half Moon Bay commented that Micron is "sampling products based on TSVs" and that "Mass production for TSV-based 3-D chips are slated for the next year or 18 month.

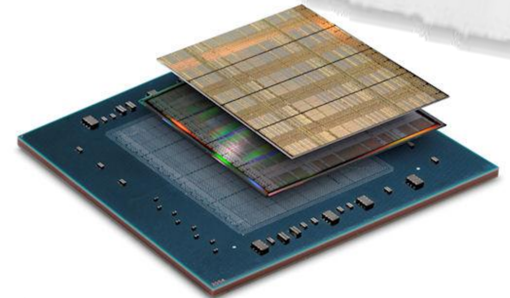


EE Times

Perfecting the 3-D chip

R. Colin Johnson
10/11/2011 10:31 AM EDT

You've heard the hype: The foundation of semiconductor fabrication will be transformed over the next few years as multistory structures rise up from dice that today are planar. After almost a decade of major semiconductor engineering efforts worldwide aimed at making the structures manufacturable, three-dimensional ICs are poised for commercialization starting next year—several years behind schedule.



COMPUTERWORLD

July 15, 2011 - 5:37 A.M.

Apple's A6 processor: 28-nm, 3D IC and made by TSMC

By Jonny Evans

While we wait for Lion, interesting to note the next Apple [AAPL] A6 processor will be made by Taiwan Semiconductor Manufacturing Co. (TSMC) and will be a 3D IC 28-nanometer low-power powerhouse, sweetly tucked inside your iPhones and future model iPads.

Silicon Valley
MercuryNews.com

New efforts to extend Moore's Law

By Steve Johnson

Continually needing to add computing power to its microprocessors, Santa Clara behemoth Intel (INTC) this year announced it was venturing beyond its traditional method of cramming more and more transistors into a flat pieces of silicon in favor of a different approach -- building chips in three dimensions.

THE WALL STREET JOURNAL.

October 25, 2011, 10:50 AM ET

Xilinx Says Four Chips Act Like One Giant

By Don Clark

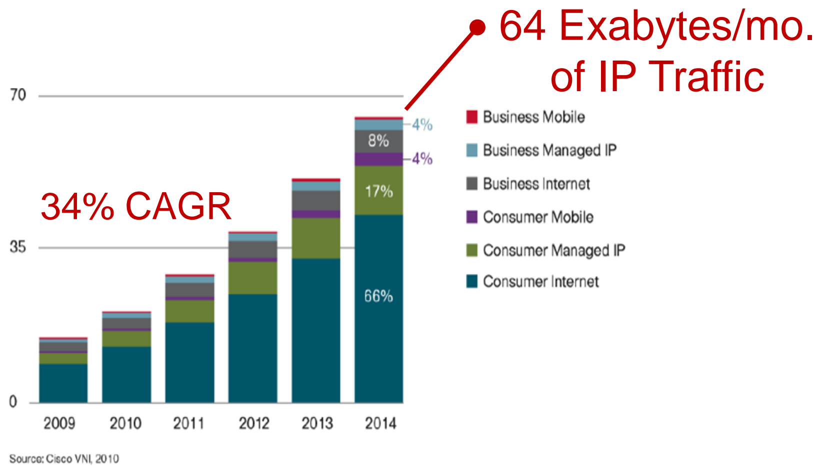
Chip makers have been living by Moore's Law for decades. But that pace of progress is not fast enough for some people, and Xilinx thinks it can help.

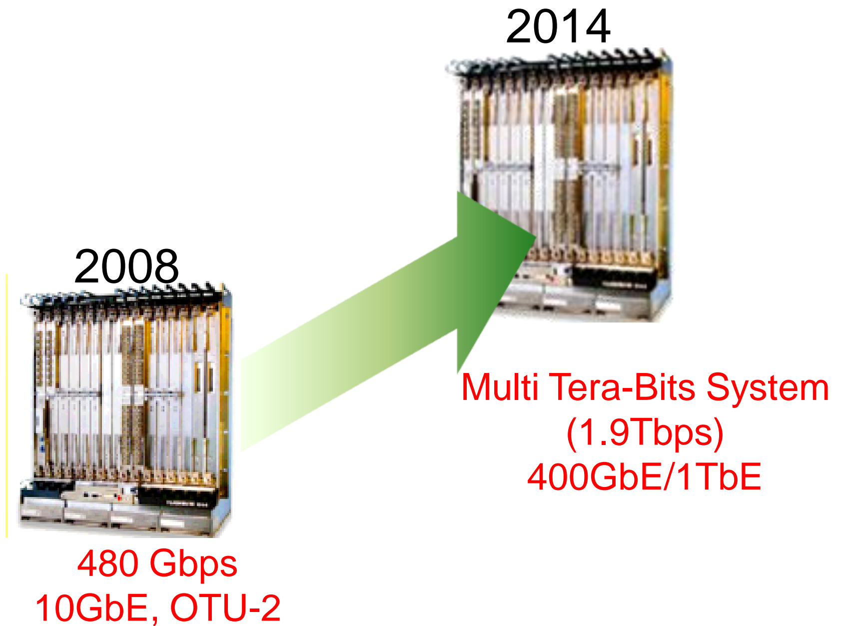
Intel co-founder Gordon Moore, in the observation that Silicon Valley residents know by heart, predicted a relentless shrinking of the size and cost of components found on chips. Th... transistors typi...

...ght 2011 Xilinx

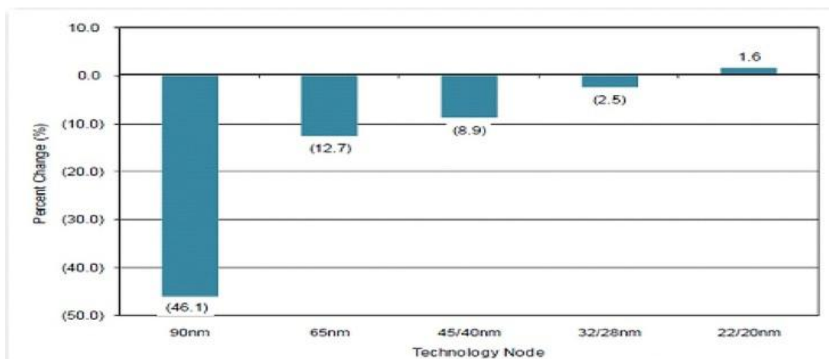
Why Now?

Market : Insatiable Bandwidth

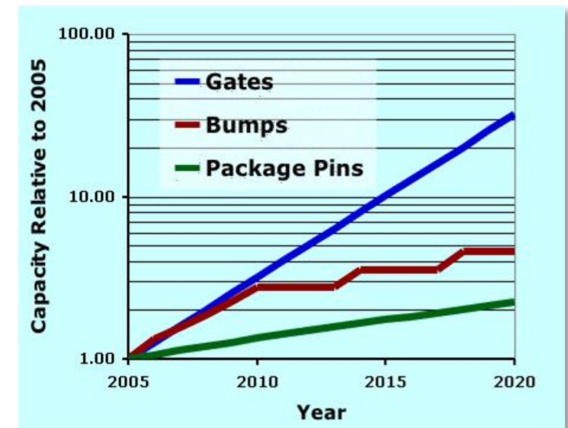




Technology : Cost, IO, Power



Source : IBS



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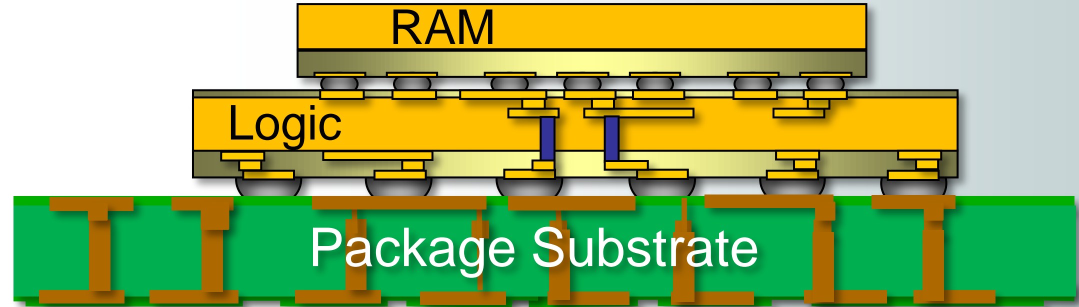
What Does 3D Buy Us?

- Connectivity
- Capacity
- Crossovers



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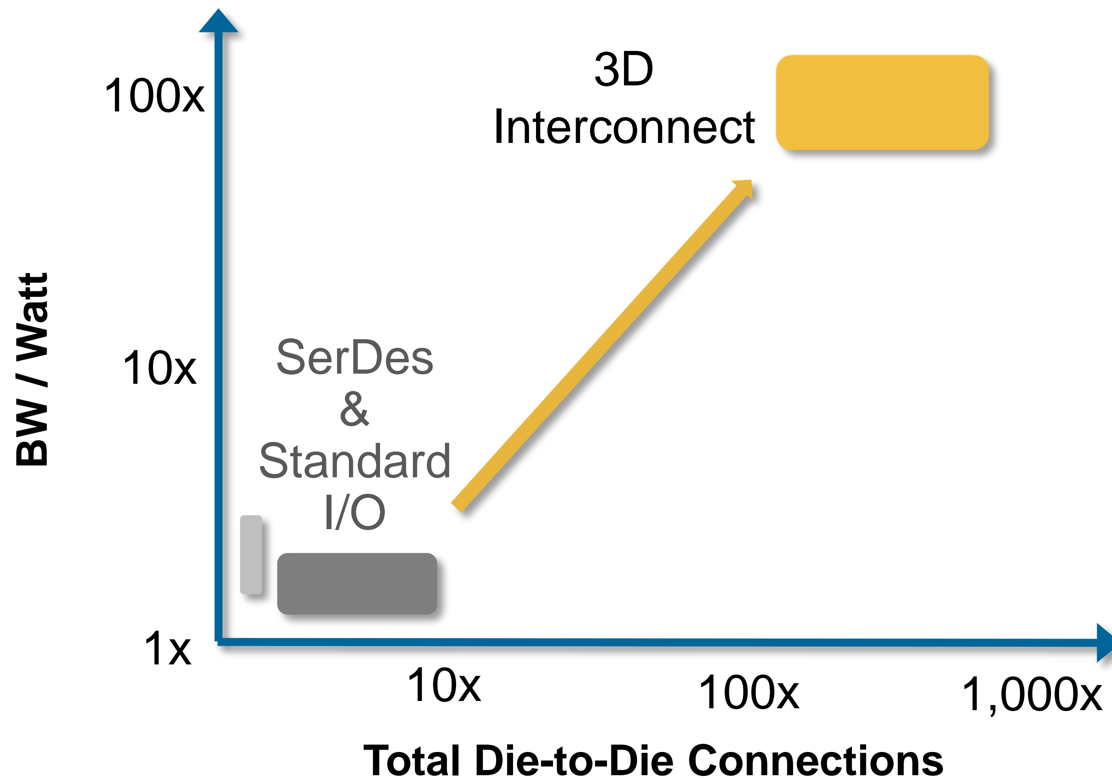
Connectivity: Enables High Bandwidth, Low Power Die-to-Die Communication



100x bandwidth/watt advantage over conventional methods

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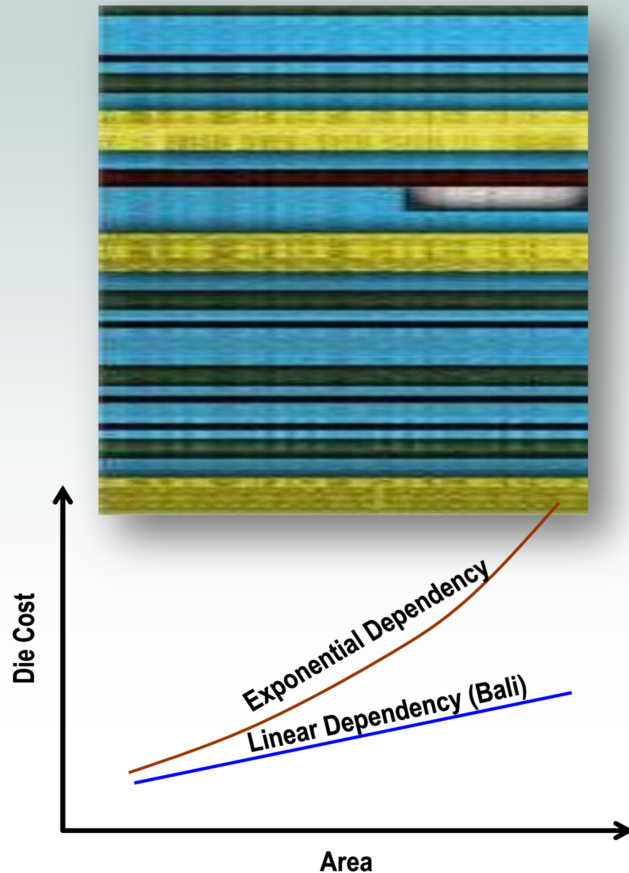
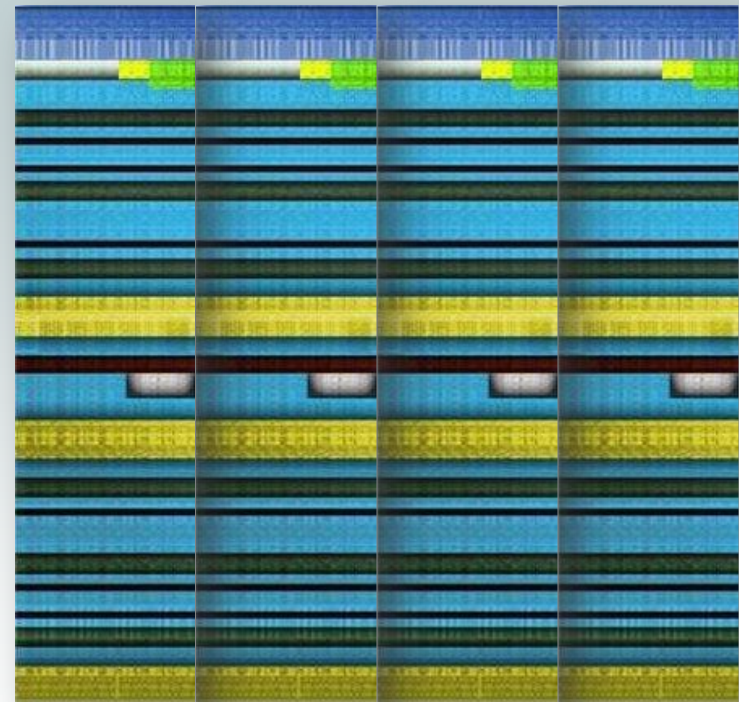
Capacity Beyond Moore's Law

Big Single Monolithic Die



Multiple Small Die Slices



✓ **Greater capacity, faster yield ramp**

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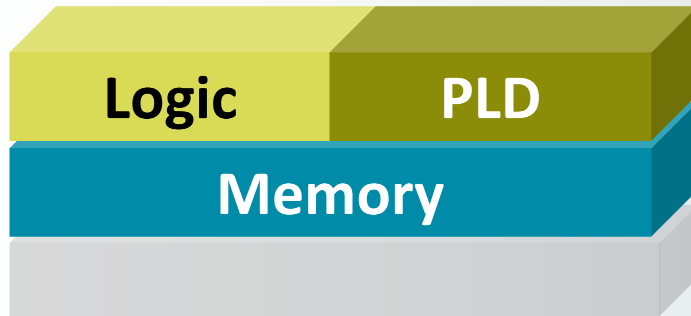
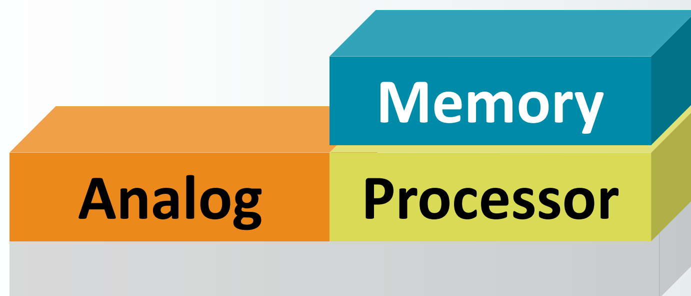
"Crossover SoCs" with Heterogeneous Die



✓Mixed functions



✓Mixed processes

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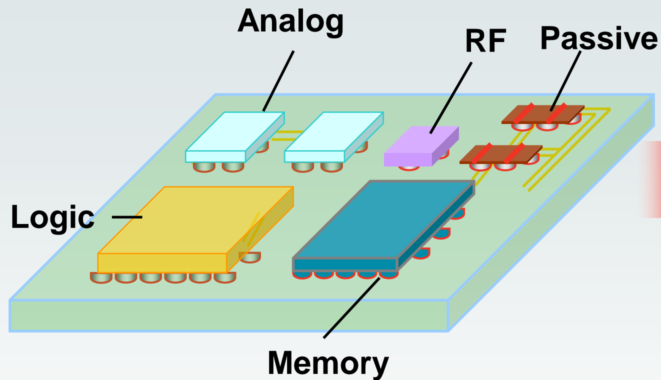
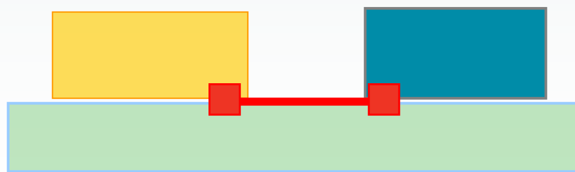
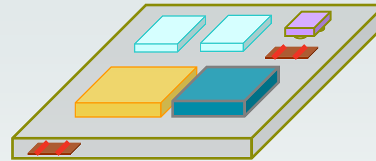
The Progression of 3D Technology

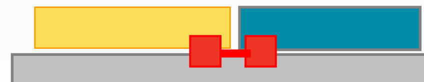
Traditional MCM/PCB	Silicon Interposer 2.5D	Full 3D



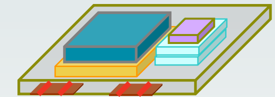


Flipchip + wire bond





2.5D side-by-side integration with TSVs & silicon interposer



Vertical stacking with memory & logic

Source: TSMC

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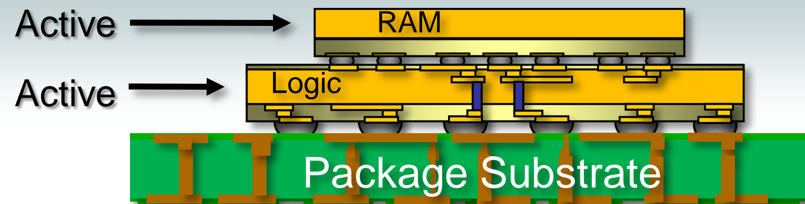
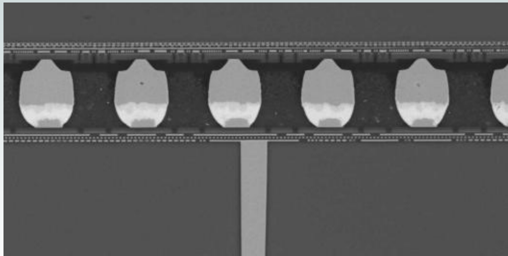
Technical Challenges Posed by 3D

3D – Active on Active

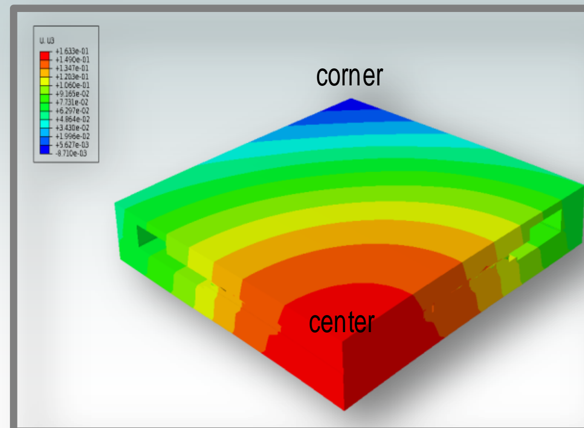
Vertical Die Stacking



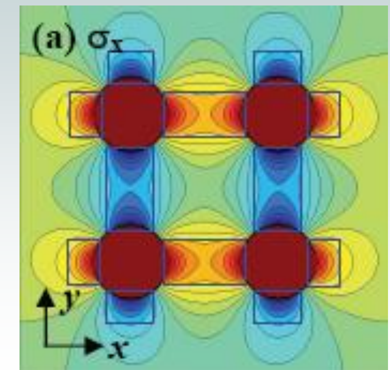
Microbump / TSV



Thermal



TSV-Induced Device Stress



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3D versus 2.5D

	3D	2.5D
Design Flow	New Co-Design	Evolutionary
Testing	New Methods	Evolutionary
Cost	High	65nm Interposer
Thermal	Challenging	Evolutionary
Device Impact	Stress	None
Reliability	Challenging	Evolutionary

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Case Study: The First 2.5D FPGAs

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Why FPGA

- **Technology**
  - Column based ASMBL Architecture
  - Large Die Integration
  - Rich Uniform Programmable Interconnect
  - Tens of Thousands of Microbumps
  - Testability
- **Application Domain**
  - Telecom
    - 400Gb Ethernet
    - Wide Data path Packet Processing
    - Highly Parallel DSP processing
  - Highest IO BW (1Terabit/sec by 2014)
  - Growing LC capacity (2 M Logic Cells)

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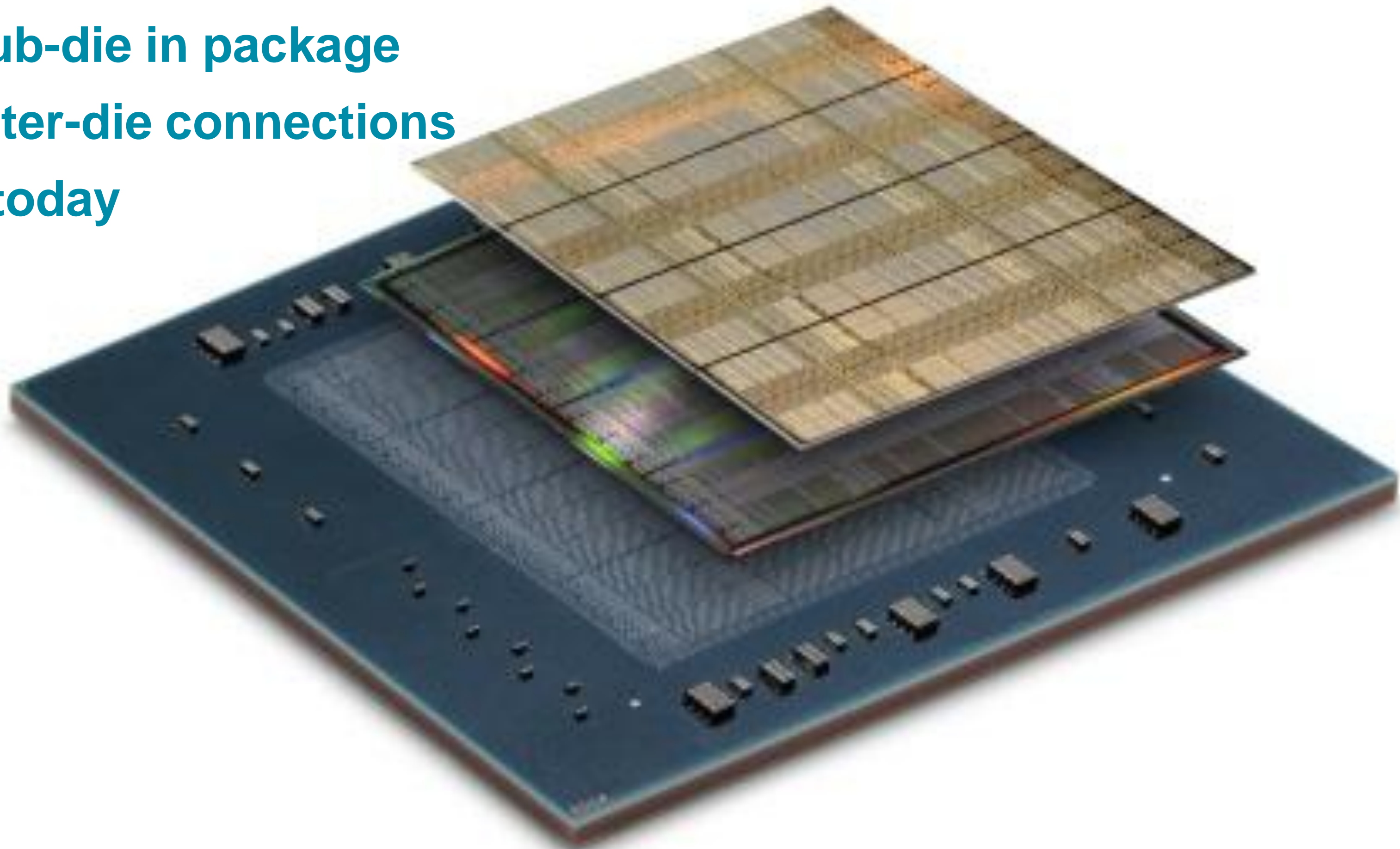
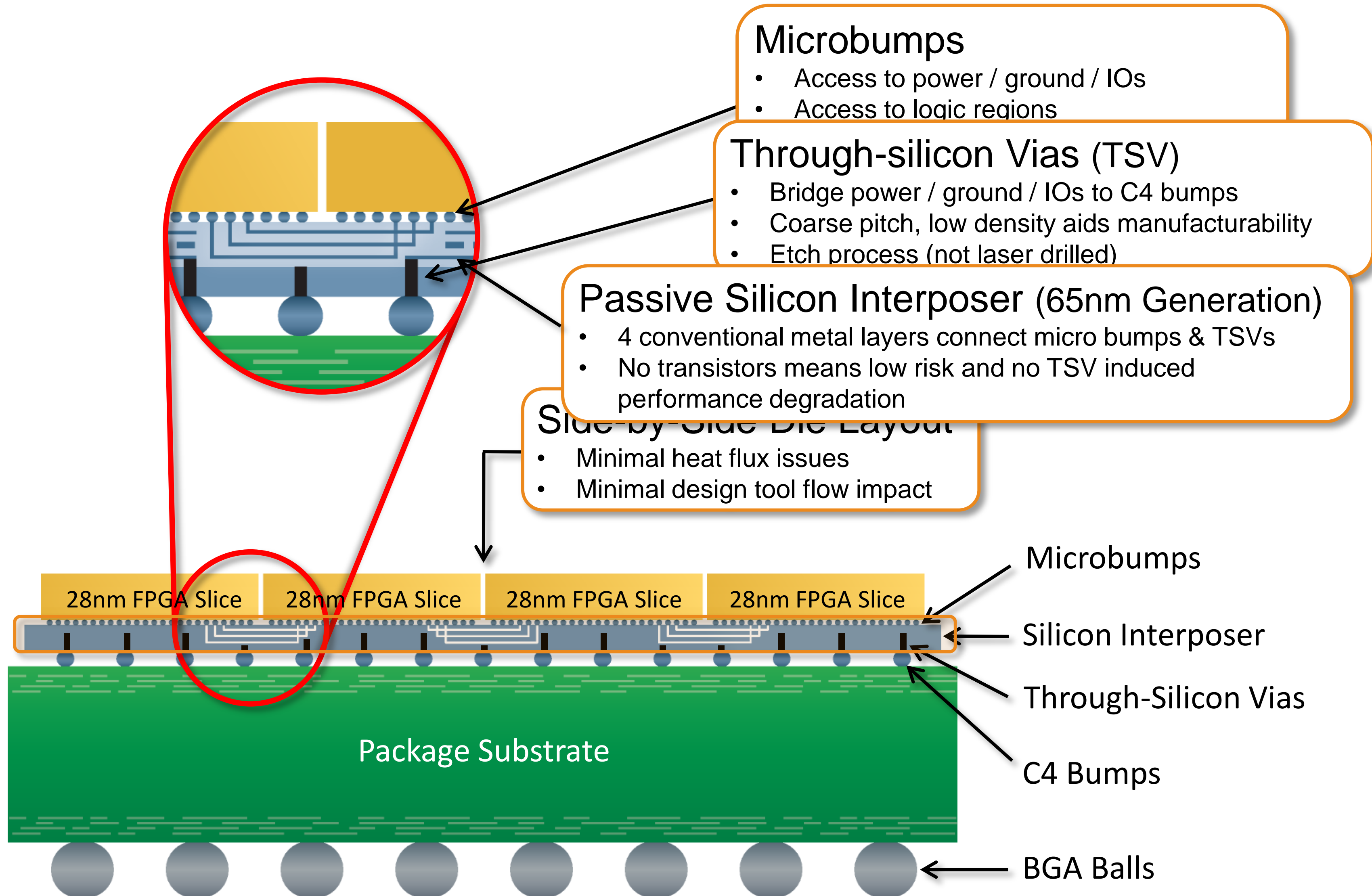
Virtex-7 2000T

- Virtex 2000T – 2 million logic cells
- 4-layer metal Si interposer with TSV
- 4 FPGA sub-die in package
- >10,000 inter-die connections
- Shipping today



Harnesses Proven Technology in a Unique Way



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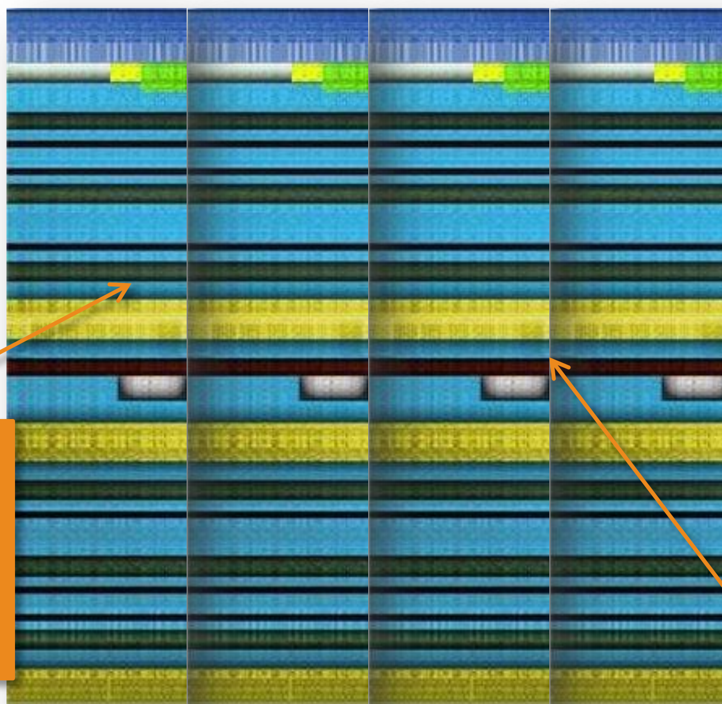
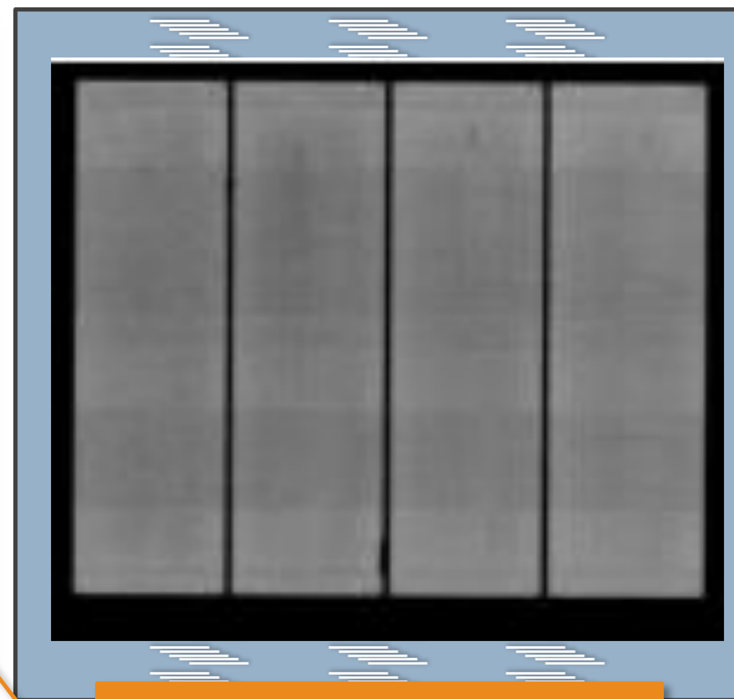
Column Based ASMBL Architecture



FPGA Slices Side-by-Side
Segmented Routing
High Yields Early



Silicon Interposer

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Advantages vs. Large Monolithic FPGAs:
Capacity and Bandwidth and Power

20W
8W
20W

980K Monolithic FPGA

980K Monolithic FPGA

8W
8W

980K Monolithic FPGA

980K Monolithic FPGA

20W
8W
20W

1 Virtex-7 2000T = **4 Largest Monolithic FPGAs**

19 Watts **112 Watts**

Bandwidth No Equivalent

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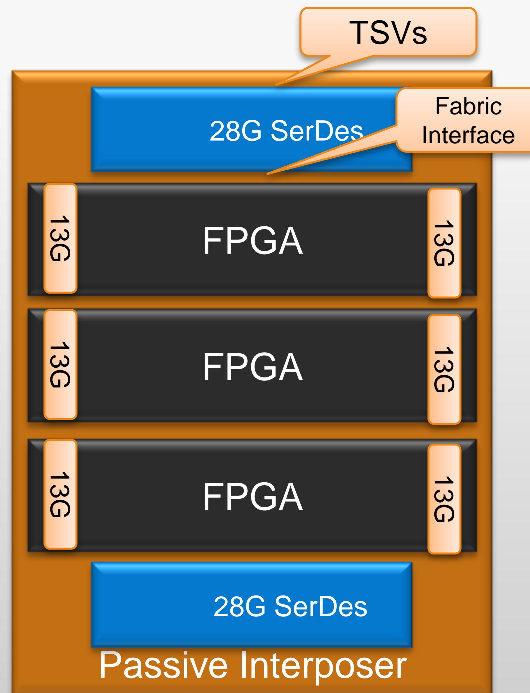
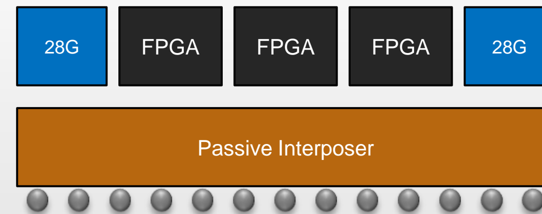
Virtex-7 HT: Heterogeneous 2.5D

Top View



- 2.8Tb/s ~3X Monolithic
  - 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 GPIO

Cross Section



- Yield optimized
- Noise isolation
- 28G process optimized for performance
- FPGA process optimized for power

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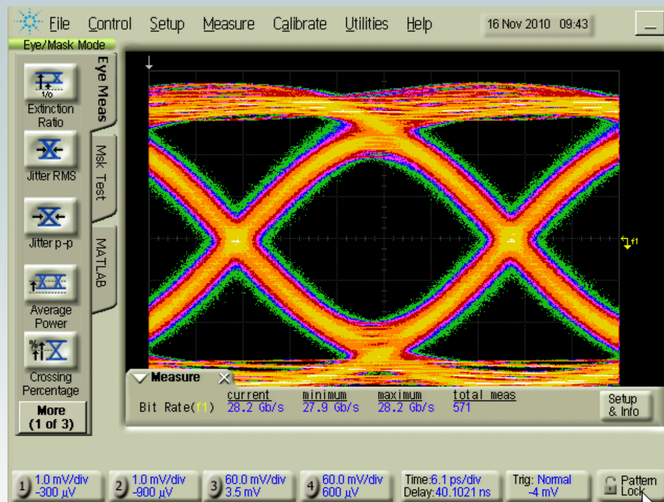
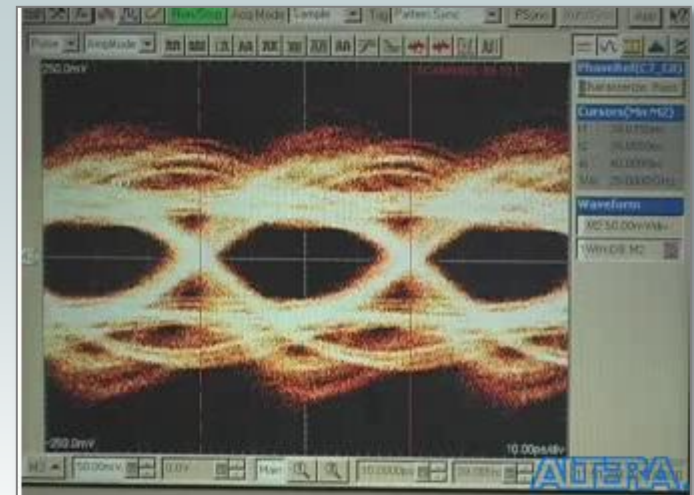
Eye Comparison: 2.5D vs. Monolithic

2.5D Virtex-7 HT @ 28Gbps



Other Monolithic FPGA @ 25Gbps



Parameter	Virtex-7 HT	Other Monolithic FPGA
Data Rate	28Gb/s	25 Gb/s
Data Pattern	PRBS31	PRBS7
Eye Opening	>2X more	Less than ½
Signal Quality	Clean Jitter	Noisy

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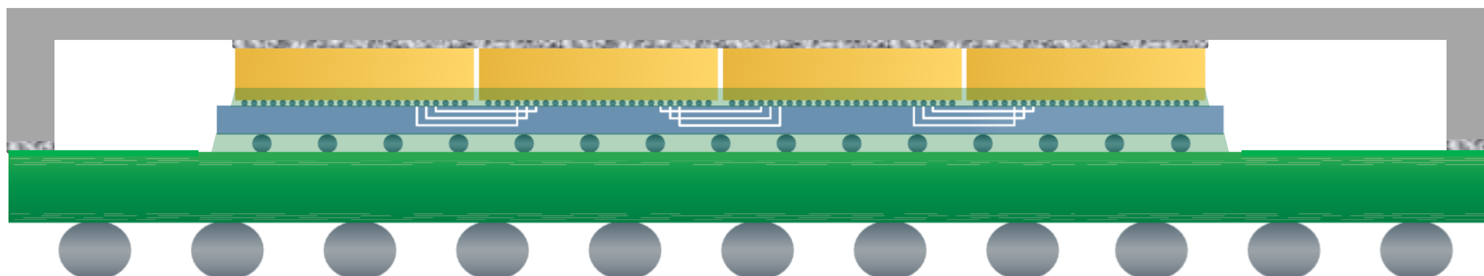
Evolutionary Technology



	SSI Package	Standard Monolithic Flip Chip
Lid	Standard (Cu – Ni Plating)	Standard (Cu-Ni Plating)
TIM	Standard (Silicone)	Standard (Silicone)
uBump	Cu Post + Lead free Solder	NA
Chip to interposer underfill	Capillary UF	NA
Interposer	65 nm Si Technology	NA
C4 Bump	SnPb	SnPb
C4 Underfill	Capillary UF	Capillary UF
Package substrate	Standard (low-CTE Core)	Standard

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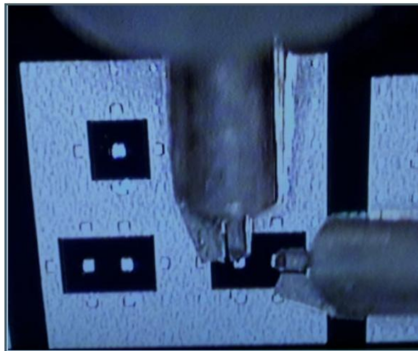
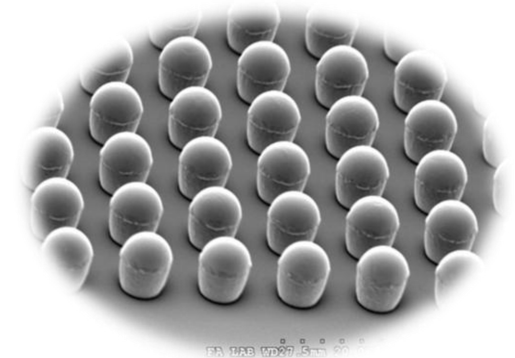
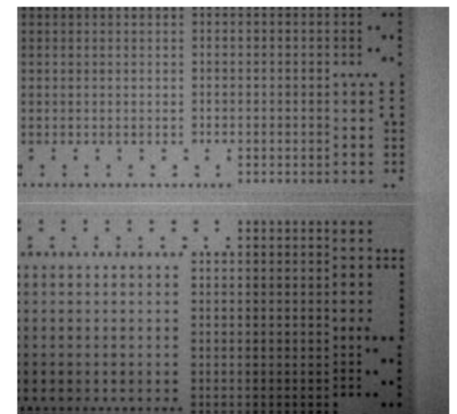
Challenges and FPGA Solutions

- Testing
  - Challenge : Probing Microbumps
  - Solution : Programmable Interconnect





- Thermal
  - Challenge : Thermal Conductivity
  - Solution : Uniform Spreading of Microbumps



- Design Flow

  Leverage Segmented Routing Architecture

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Creating the Supply Chain

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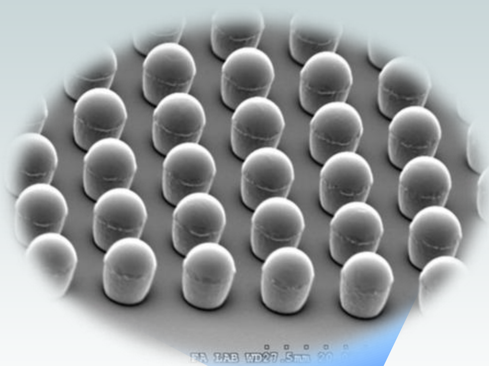
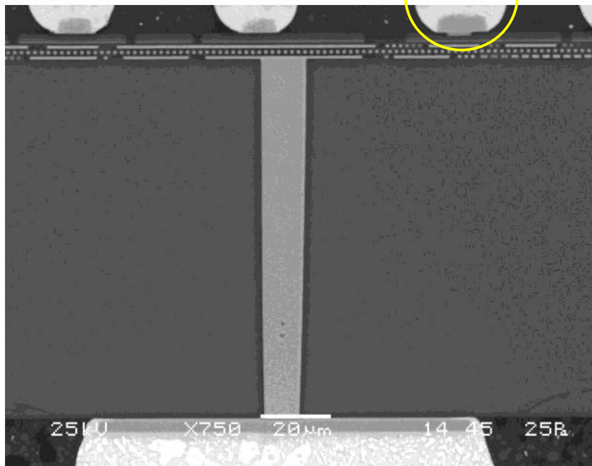
Assembly Options Considered

TSV via and Microbumps

Source: Xilinx, TSMC, Amkor





Die to Die

- **#1 M.Reflow + CUF**: Die to Die Attach → Reflow → Capillary Underfill → Die Stack to Substrate → Reflow → Capillary Underfill → Final Test
- **#2 TC Bond + CUF**: Die to Die TC Bond → Capillary Underfill → Die Stack to Substrate → Reflow → Capillary Underfill → Final Test
- **#3 TC Bond + NCP**: Die to Die TC + NCP → Die Stack to Substrate → Reflow → Capillary Underfill → Final Test

Die to Wafer

- **#1 TC Bond + CUF**: Die to Wafer TC → Capillary Underfill → (Dice) → Die Stack to Substrate → Reflow → Capillary Underfill → Final Test
- **#2 TC Bond + NCP**: Die to Wafer TC + NCP → (Dice) → Die Stack to Substrate → Reflow → Capillary Underfill → Final Test

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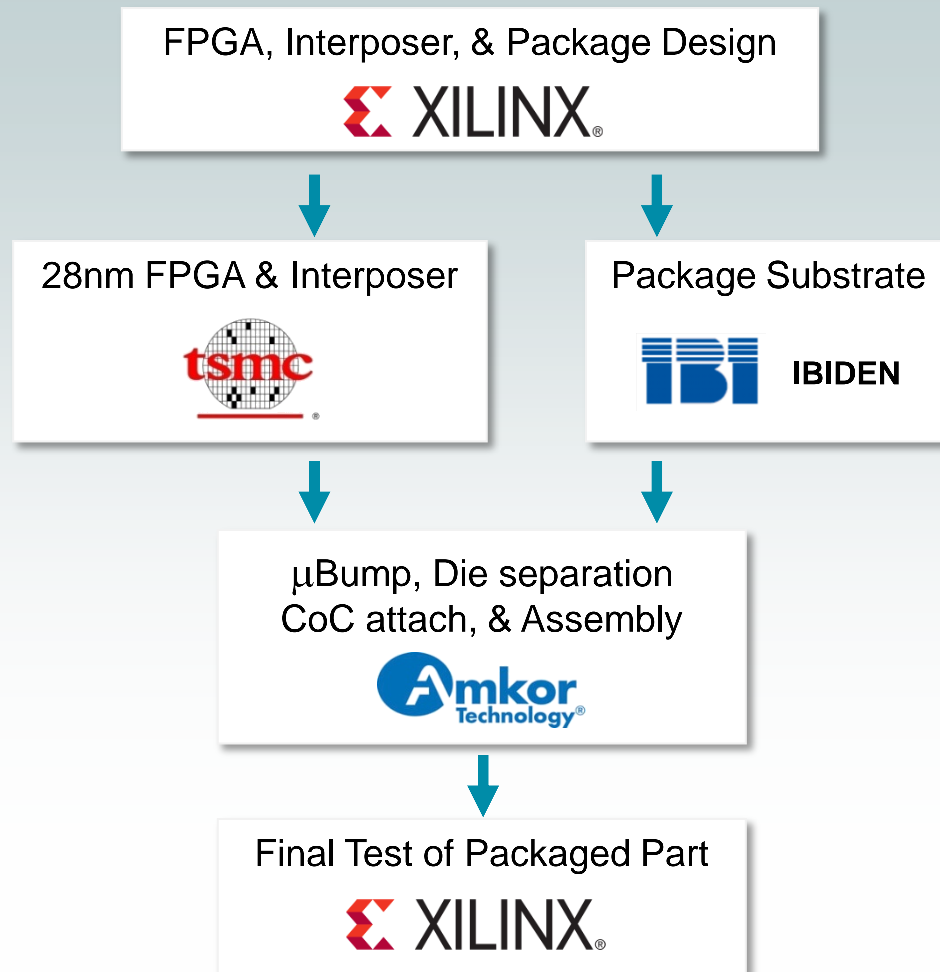
The Xilinx 2.5-D Supply Chain



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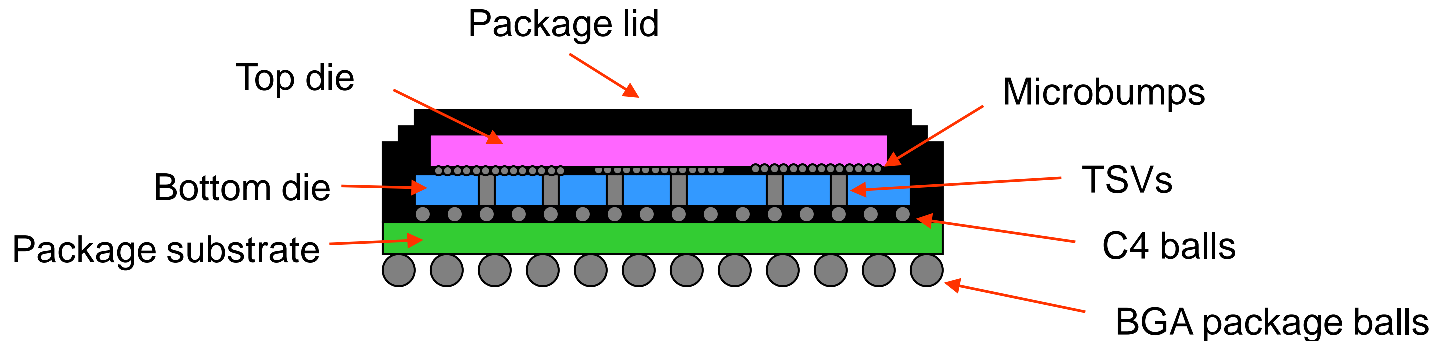
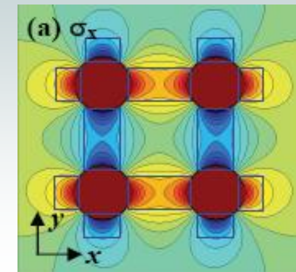
3D: The next frontier

- **Who's on top?**



- **High performance chip on on top for thermal and TSV process availability**
- **Floor-planning critical:**
  - Thermal concerns (stacked thermal flux)
  - TSV keep out zones in bottom die to avoid stress induced performance impact

TSV-Induced Device Stress



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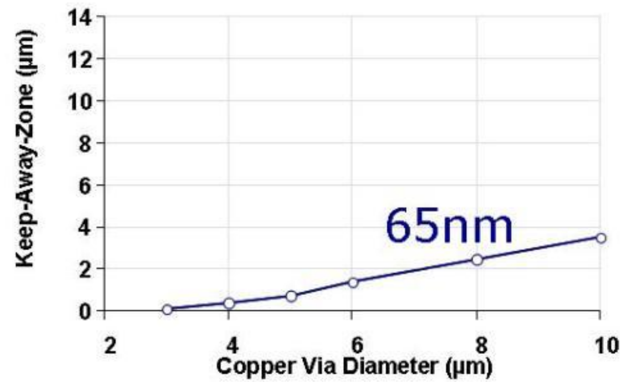
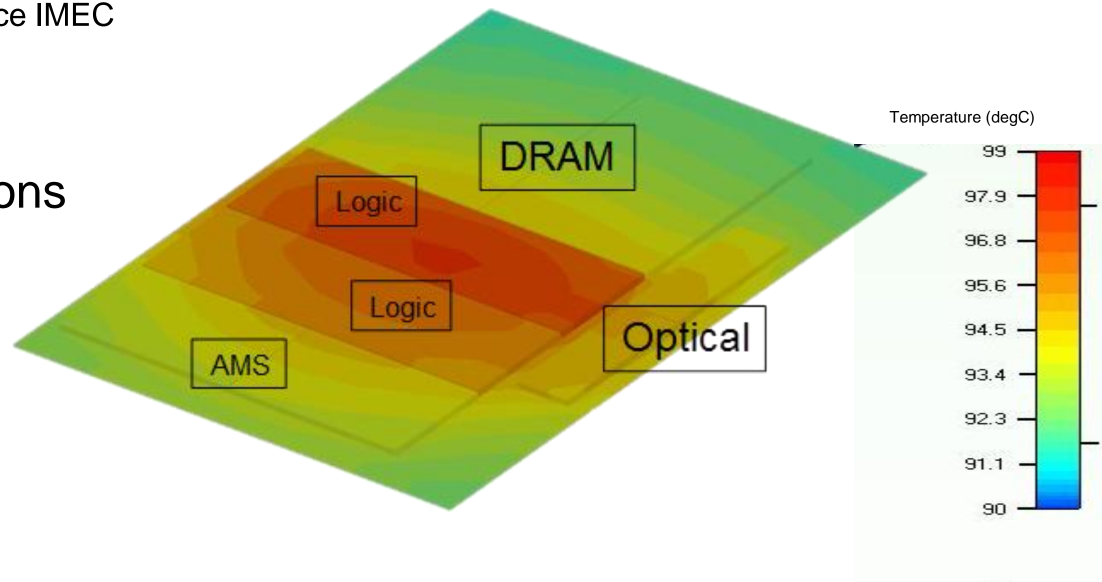
3D Challenges

- **Keep out zone**



Source IMEC

- **Thermal concerns**
  - E.g Optical 85C junctions



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3D Call-to-Action: Develop & Evolve Standards

- **Design enablement**
  - Models
  - 3D Process Development Kit
- **Manufacturing standards**
  - DFM rules for TSV, microbump (AR, keep-out)
  - Materials TSV, u-bump
  - Thermal budget
- **Test**
  - Test HW
  - KGD method
  - u-bump probing
- **Interoperability of silicon between fabs**
  - Shipping methods
- **Chip-to-chip Interfaces**

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3D Eco System

- ✓ Leading fabless & fablite companies
- ✓ Equipment manufacturers
- ✓ Fabs and OSAT
- ✓ Industry consortia

- Requirements alignment
- Industry standards setting
- Best practice sharing

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Summary

✓3D ICs are here!
- Significantly changing the semiconductor landscape

✓Challenges remain
- Technical and business-related

✓2.5D is here to stay
- An important & lower risk path

✓3D Call to action
- Industry standards are badly needed

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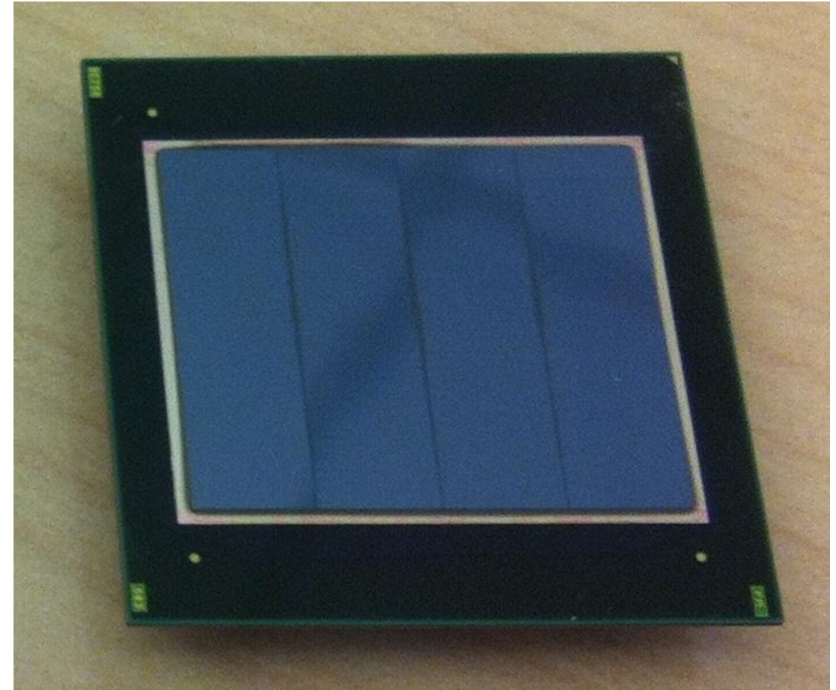
Stacked Silicon Interconnect: A world of difference



Earth
Area: ~500 Million km^2
Population: ~6.8 Billion People
Oceans: 5
Age: 5 Billion Years

Virtex-7 2000T
Interposer Area: ~775 mm^2
Population: ~6.8 Billion Transistors
Chips: 5
Age: 5 weeks

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