

Blue Pearl Software to Showcase the Visual Verification Suite at the Upcoming Xilinx Developer Forums

SANTA CLARA, California –Sept. 24, 2019 – Blue Pearl Software, Inc., a leading provider of design automation software for ASIC, FPGA and IP RTL verification, announced that it is a Silver level sponsor of the upcoming [Xilinx Developer Forum \(XDF\) 2019](#), where it will showcase its Visual Verification™ Suite. The [XDF Americas](#) will take place October 1st and 2nd in San Jose, California; [XDF Europe](#) is November 12th and 13th at The Hague / Den Haag, Netherlands and [XDF Asia](#) will be held December 3rd and 4th in Beijing, China.

With the Visual Verification Suite, designers verify as they code. The suite features HDL Creator™ smart editor, Analyze™ RTL advanced static and formal linting, an integrated debug environment, enhanced Clock Domain Crossing (CDC) analysis and automated SDC generation. An integrated Management Dashboard is also provided to track progress and deliver signoff statistics for audits and design reviews.

“We have worked closely with Xilinx to integrate our verification solution and today the Visual Verification Suite can use a Vivado Design Suite project or with our Tcl Store app, can be called from within Vivado,” said Ellis Smith, Blue Pearl Software, Chairman and CEO. “No matter the approach, visual verification enables design teams to find and fix errors faster. Stop by and see for yourself.”

More information about XDF is available at: <https://www.xilinx.com/xdp>. For additional updates from XDF, follow Xilinx on Twitter at @XilinxInc or via the hashtag #XDF2019.

Not Attending XDF 2019?

- Read our latest [blogs](#)
- Try out the [Visual Verification Suite Starter Edition](#)
- Browse the Blue Pearl [Verification Methodology Guide](#)
- [Read more](#) about the Visual Verification Suite

About Blue Pearl Software

Blue Pearl Software, Inc. is a leading provider of DO-254 compatible design automation software for ASIC, FPGA and IP RTL verification. Our customers are RTL managers and developers in military, aerospace, semiconductor, medical, communications and safety critical design companies. The Visual Verification™ Suite speeds block and project level verification with advanced integrated RTL structural and formal linting, constraint generation and clock domain crossing analysis. Our usability is unmatched in the industry and can help your design team accelerate development and produce high reliability designs. The Visual Verification Suite is designed, tested and supported in the United States of America.

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