High Speed Serial Link Simulation based on Dynamic Modeling

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Outline

- **High Speed Link Simulation Overview**

- **Static Simulation – Conventional Method**

  – **Example of unaddressed issues**

- **Dynamic Simulation Introduction**

  – **Basic concept, necessity, and implementation**

- **Dynamic Simulation Case Study**

- **Conclusions**

# High Speed Link Simulation Overview

- High speed serial link system simulation has achieved a lot in the past decade
  - Simulation scope: all EQ blocks, adaptation blocks, calibration loops, non-idealities (nonlinearity, latency, hysteresis, etc.), PND noise, crosstalk, reflections, jitter, etc.
  - Simulation methodology: Statistical, time-domain, (semi-)analytical, and various combinations to predict link performance at a low BER (e.g., <1E-15).

- IBIS-AMI modeling gains its popularity
  - Allows one vendor's IP to be co-simulated with another's.
  - Relies on specific EDA vendor's pre- and post- processing.

Static Simulation

Case Study

Static Simulation – case description

- ## Simulation is essentially "static"
  - Although CDR timing and equalizer settings are changing with time, link parameters and silicon behaviors are not.
  - As a result, some performance impact might not be covered in simulation, resulting in improper decisions for product development.

- ## An example of a real product problem
  - Both simulation and lab test showed that the system ran with margin at -20°C, 25°C, and 80°C.
  - Temperature ramping test showed that
    - When system started at low temp, errors could show up anywhere above 70°C.
    - When system started at high tem, the temp ramping test went error-free.
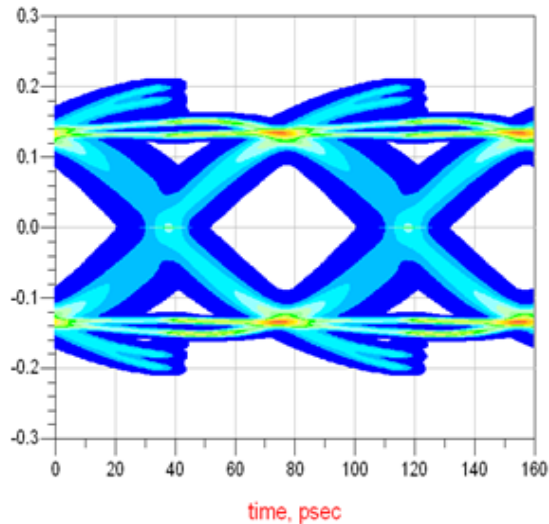

Temperature profile
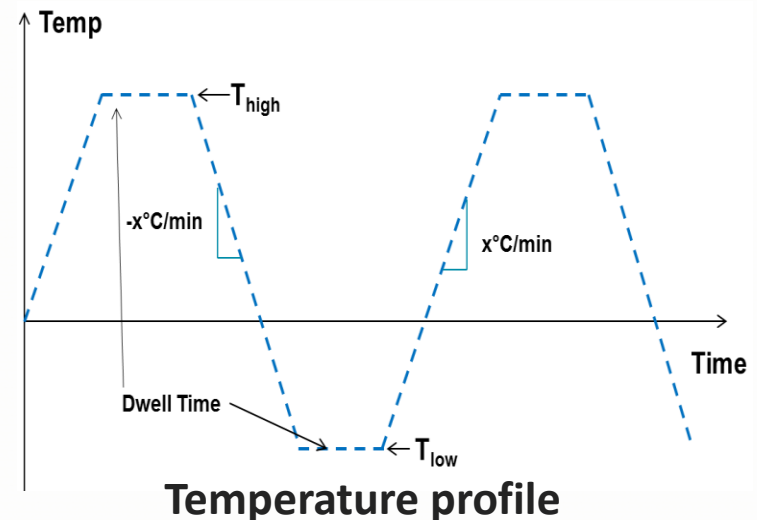
System Configurations

- More than 6dB in insertion loss between -20°C (blue) and 80°C (red) are experienced for 12.5Gbps.

- SerDes includes TX 3-tap FFE (programmable), RX CTLE (auto-tuned then fixed), and RX DFE (adaptive).

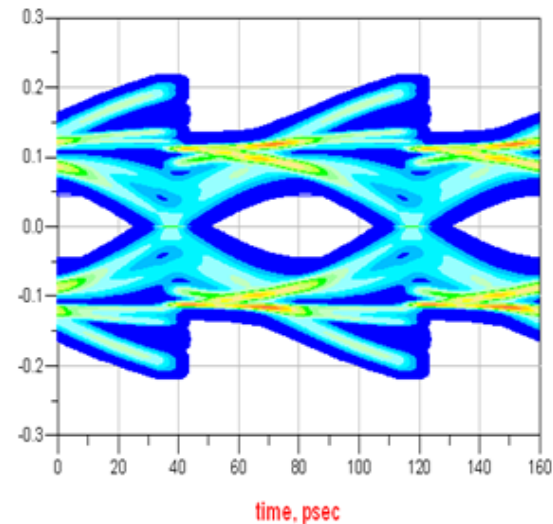- TX swing is constant and output eye is shown below:
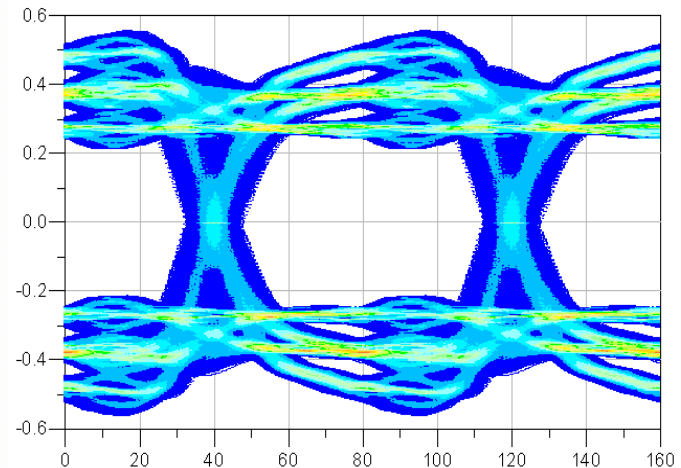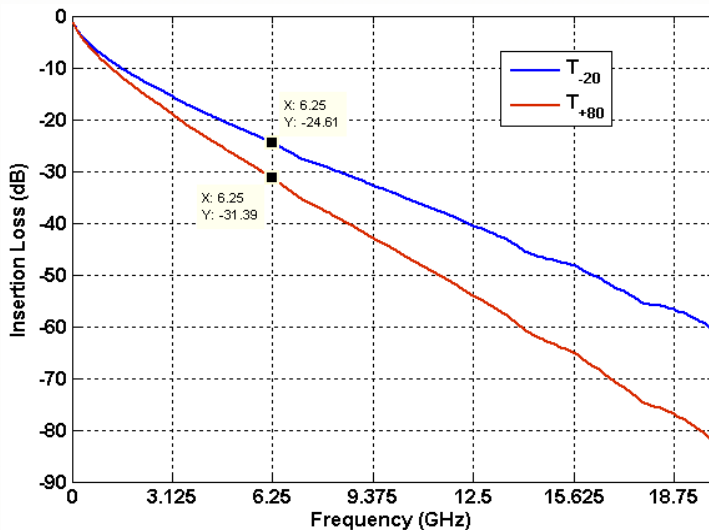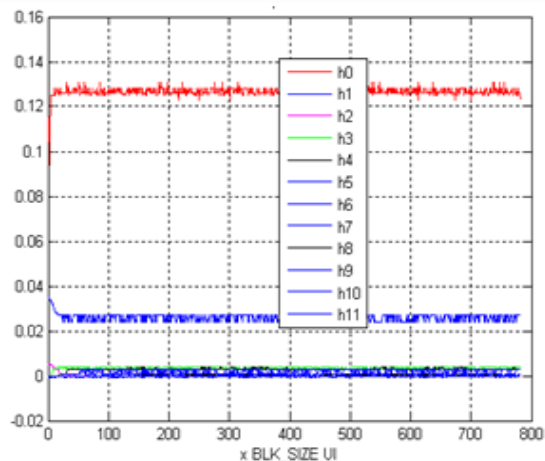
System Started at Low Temperature
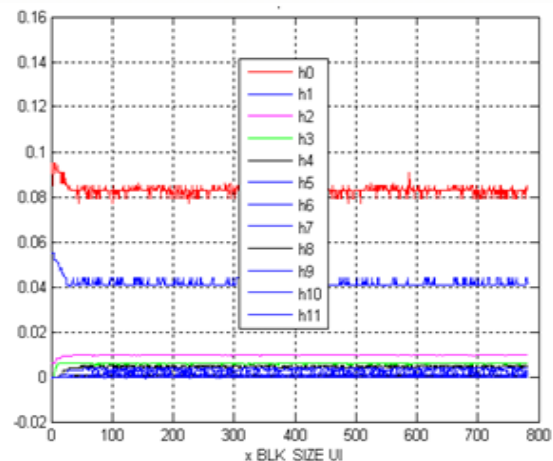

Eye at low temp with BER=8.78E-36

Eye at high temp with BER=3.37E-13

Converged DFE settings for low temp

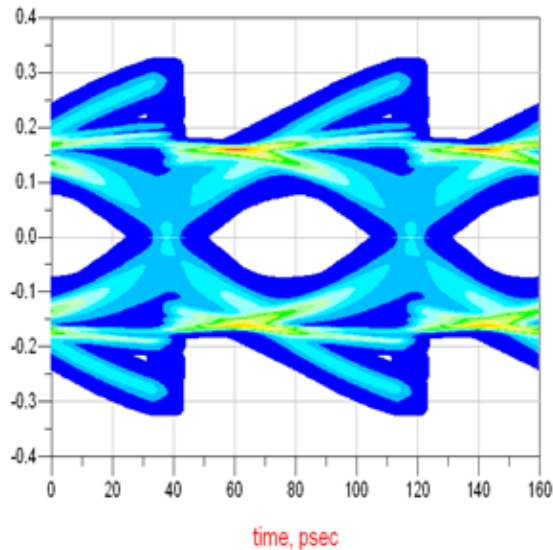Converged DFE settings for high temp

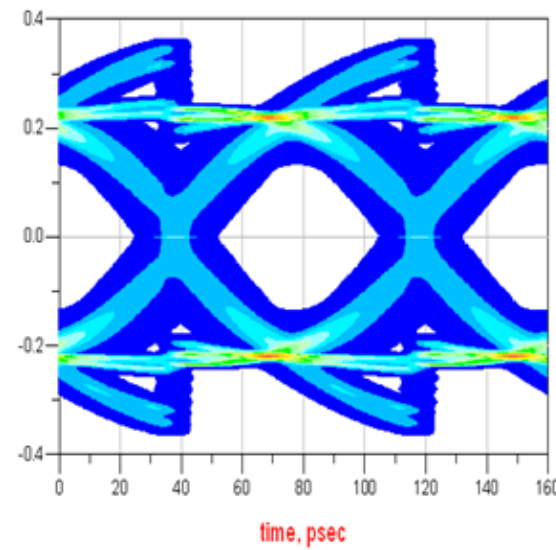DESIGNCON 2014

Observations – 1

- When the system is started at low temp, the CTLE (Peaking and Boost) are auto-tuned; the system shows a good margin.

- When the temperature increases to 80°C, the channel loss increased by >6dB. Because CTLE does not change, it does not

    - provide adequate equalization, leading to much higher relative values of h1 and h2 with respect to h0.

    - provide enough Boost, leading to smaller h0: h0 settles around 90mV, instead of 130mV as shown for the low temp.

- As a result, when the system is started at low temp, it loses a lot of margin at high temperature, due to the fact in this design the CTLE does not continuously adapt.

    - This correlates with lab observations.
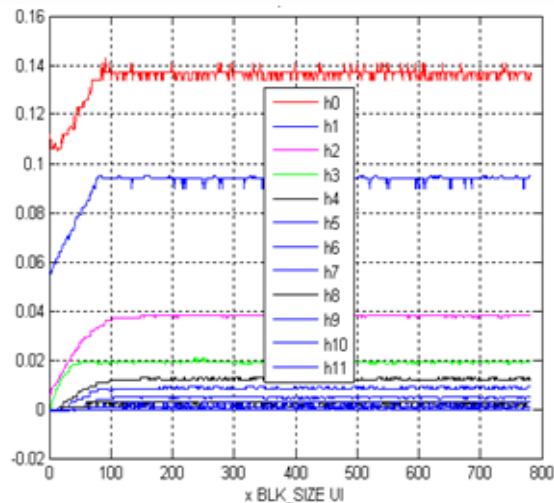
System Started at High Temperature
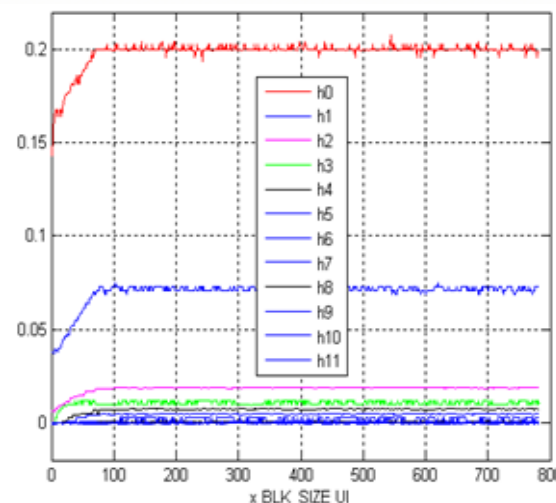
Eye at high temp with BER=6.32E-20

Eye at low temp with BER=2.51E-27

Converged DFE settings for high temp

Converged DFE settings for low temp

Observations – 2

- When the system is started at high temp, the CTLE (Peaking and Boost) are auto-tuned for the given channel characteristics. The system shows a good margin.

- When the temperature decreases to -20°C, the channel loss becomes less, making the signal stronger reaching the RX.

  - The h0 value is larger and DFE tap coefficients are smaller, implying less ISI cancelation work is required from the DFE.

  - Even though the CTLE was tuned at high temp, at low temp the system actually achieves more performance margin.

- At both temperature extremes the system is robust in performance.

  - This correlates with lab observations.

Dynamic Simulation Concepts and Examples

Dynamic Simulation Concept

- Environmental change impact on system is not well modeled by static simulation practiced in the industry.

- Environmental change not only affects interconnect characteristics, but also affects silicon behaviors.

- Equalization, etc., parameters not only depend interconnect characteristics, but are also inter-related.

  – Static simulation has the initial conditions fixed.

  – Dynamic simulation uses changing initial conditions.

- A series of static simulations do not always equal to the proposed dynamic simulation.

Implementation Considerations (1)

- Example of modeling backplane parameter change:

  ❑ Using a FIR filter to represent a passive link channel

  ❑ An example how FIR-tap coefficients are arranged

 ❑ The key is to assure no glitches are introduced when switching
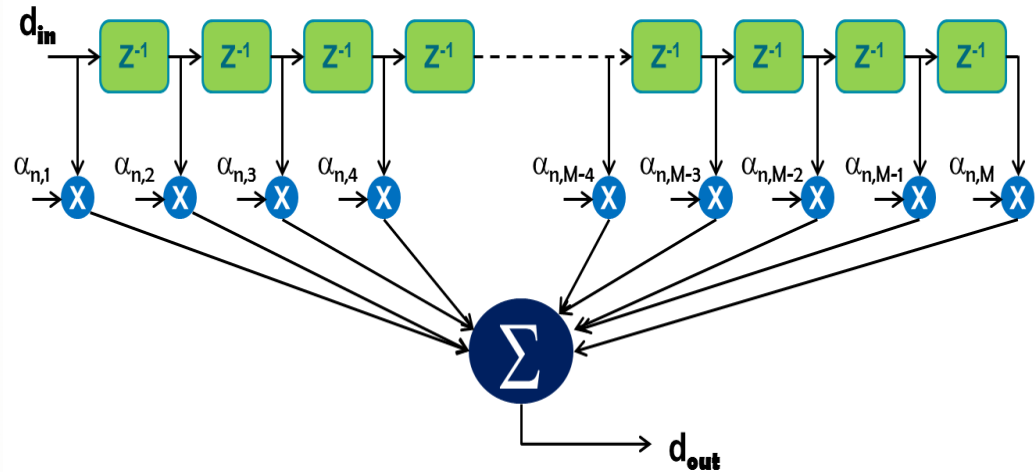
FIR_1	$\alpha_{1,1}$	$\alpha_{1,2}$	$\alpha_{1,3}$	...	...	...	...	$\alpha_{1,M-1}$	$\alpha_{1,M}$
FIR_2	$\alpha_{2,1}$	$\alpha_{2,2}$	$\alpha_{2,3}$	...	...	...	...	$\alpha_{2,M-1}$	$\alpha_{2,M}$
...	...	...	...	...	...	...	...	...	...
FIR_N	$\alpha_{N,1}$	$\alpha_{N,2}$	$\alpha_{N,3}$	...	...	...	...	$\alpha_{N,M-1}$	$\alpha_{N,M}$

# Implementation Considerations (2)

- Example of modeling CTLE (one stage) is the following:

  - It involves at least two dimensions, change as a function of time and different settings, not to mention supply impact.

  - For the settings any time 3 have to be included in the simulation. They change dynamically.

    - The group, (k-1, k, k+1), will move up or down together, unless setting limit is met
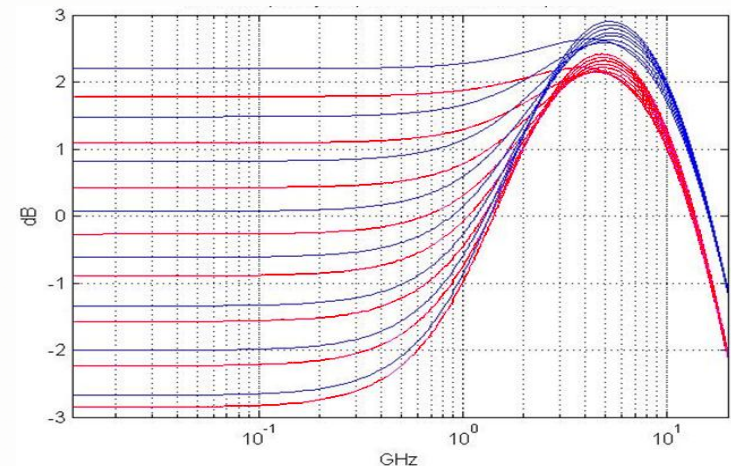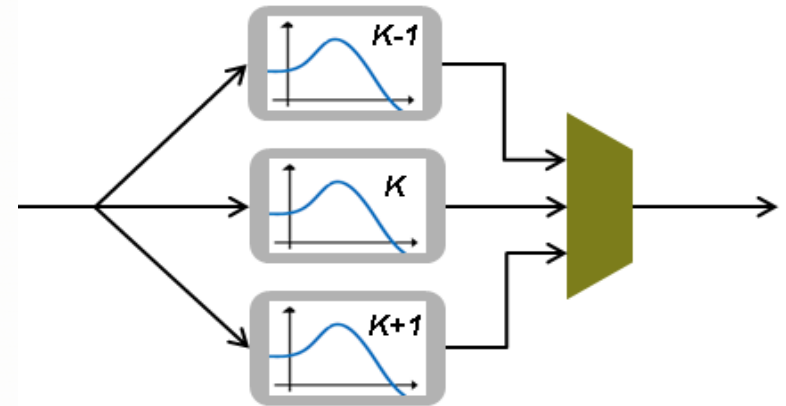
Dynamic Simulation Example

- System is running at 10Gbps.
- The environment temperature range: -25°C to 85°C.
  - Choosing 10°C step size to represent the system
- Blocks modeled as functions of temperature include:
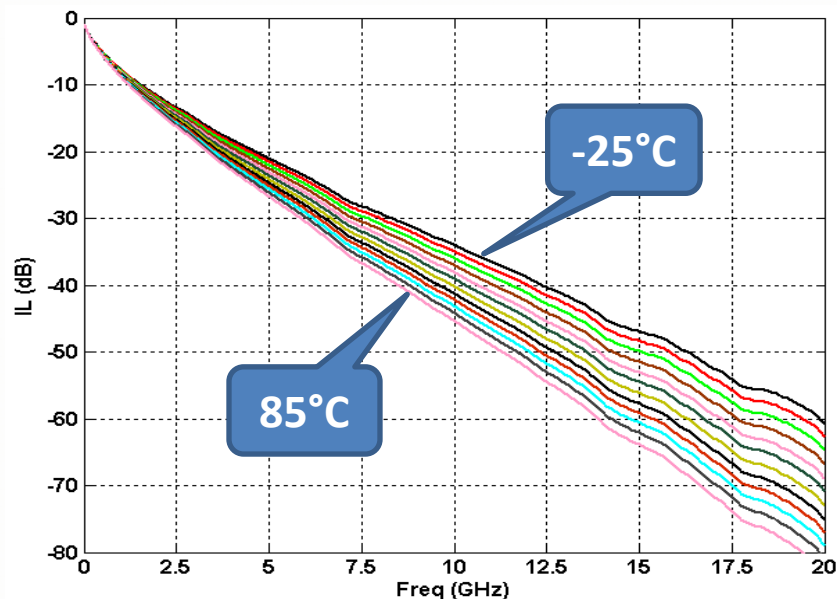
| Modeled Blocks |
|---|
| TX driver bandwidth |
| RX front-end bandwidth |
| CTLE transfer functions |
| DFE loop |
| CDR loop |
| Latch offset |
| Intrinsic jitter |
| Intrinsic noise |

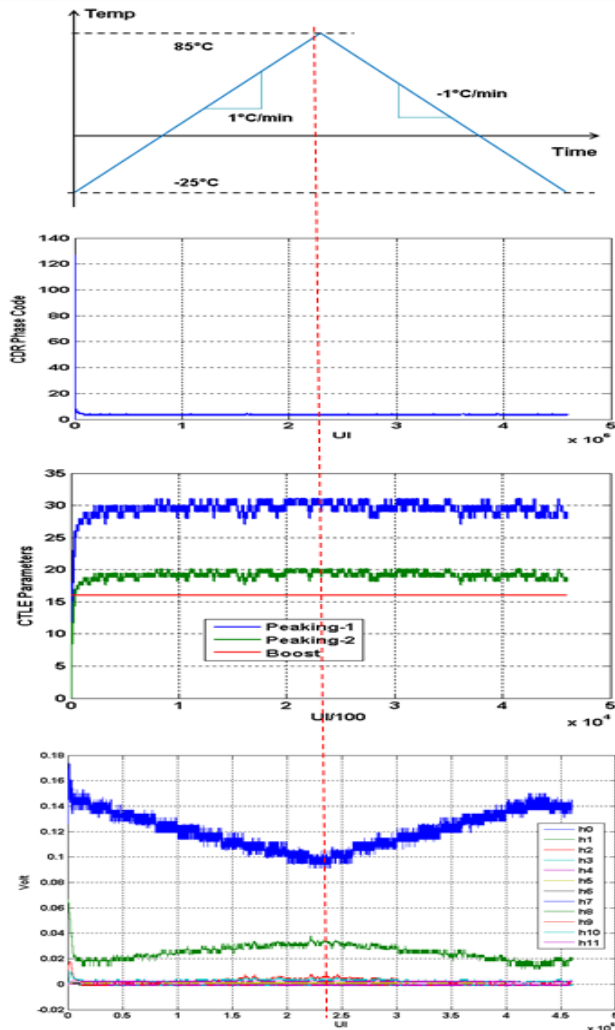# Temperature Ramping Profile

- Remove the dwell time to reduce simulation time;

- Assume the temperature of backplane and device are the same;

- Choose to map every 200K bits of simulation to 1 minute of running, resulting in a ratio of 1 to 3 million;

- we need to simulate (24-1)*200K = 4.6M bits to complete on cycle
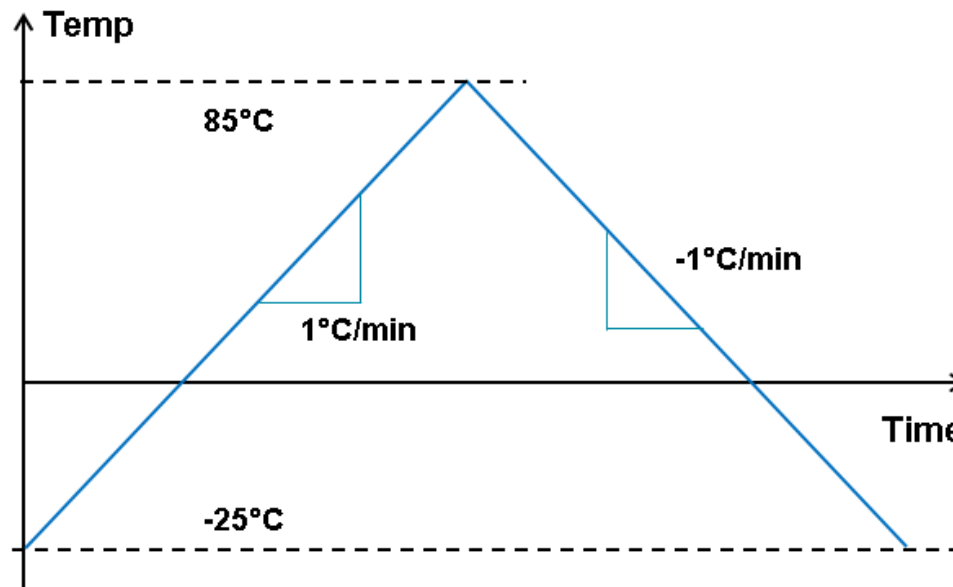
Setup Configurations

- The SerDes model has the following main blocks:
  - TX 3-tap FFE de-emphasis: $\{C_{-1}, C_0, C_1\}$;
  - RX CTLE: A boost stage and two peaking stages;
  - RX DFE: 11-taps;
- The TX de-emphasis and output swing is fixed.
- Both CTLE and DFE settings are adaptive, but will compare
  a. Boost is pre-set
  b. Boost is adaptive

Setup 1: Boost is Pre-set


- The CDR settles in a tight range, not much affected by temperature.

- h0 decreases when tem rises and climbs back when temp falls.

- The CTLE settings do not change much during temperature ramping.

- As temperature rises, h1 increases to account for more ISI from loss.

- The values of h2 and h3 are small, but do increase at high temp.

- All in all, adaptation is doing its work trying to achieve desired performance.

Setup 2: Boost is Adaptive
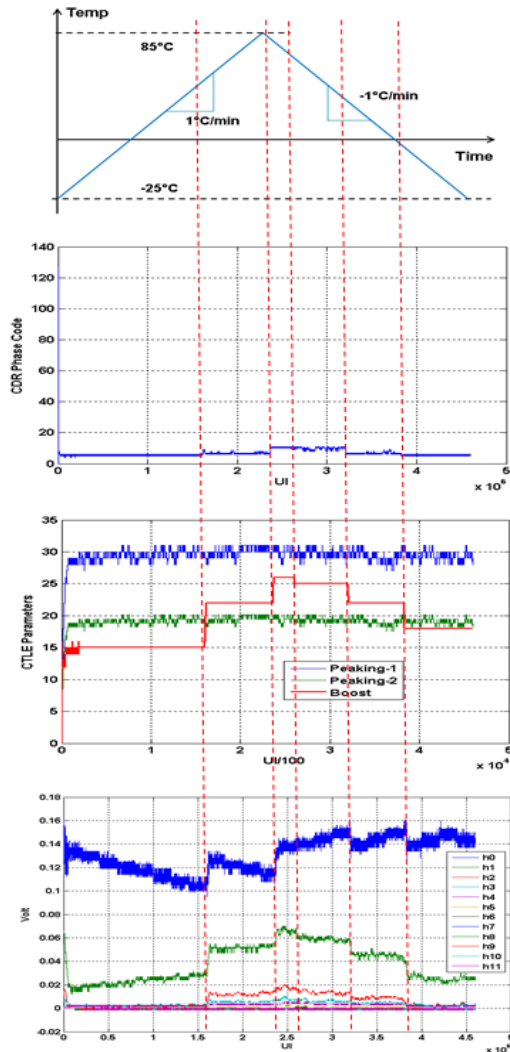
- Whenever Boost changes, the CDR also shifts accordingly.
- Signal strength, h0, is directly impacted by Boost.
- The CTLE does not change much during temperature ramping.
- h1 tracks h0 and channel loss (due to temperature) to remove ISI.
- As seen, for the same temperature, RX settings could be different.
  - This is not available in static simulations.
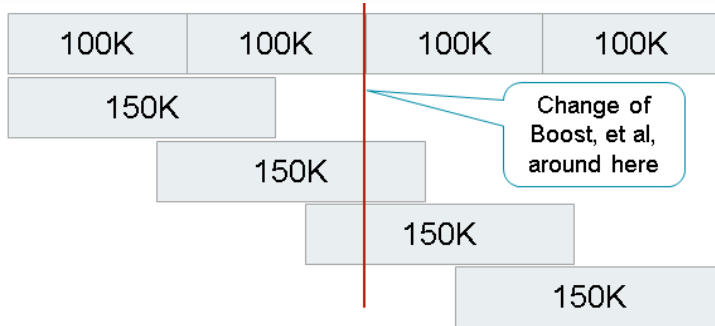
Data Eyes for the Two Setups
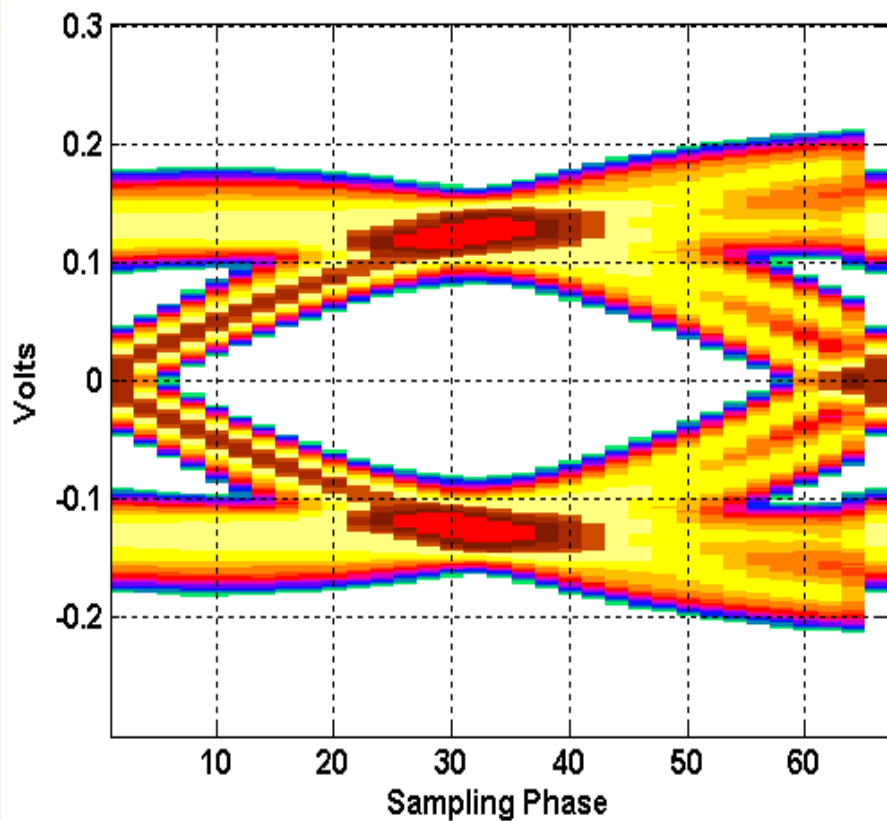

(a) Boost fixed
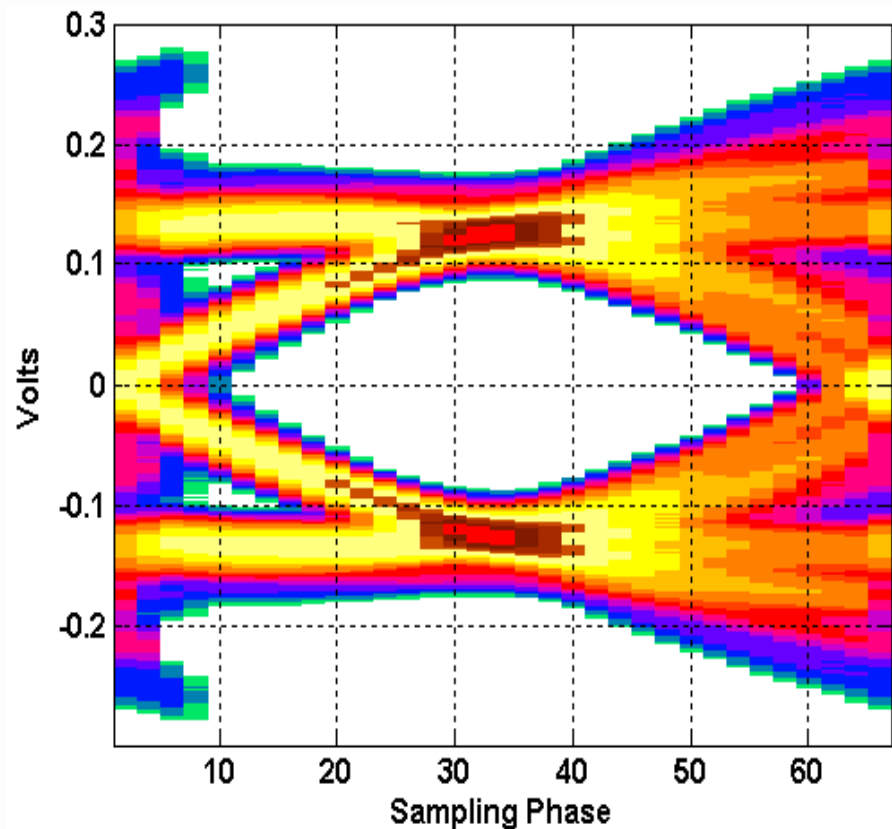
(b) Boost adaptive

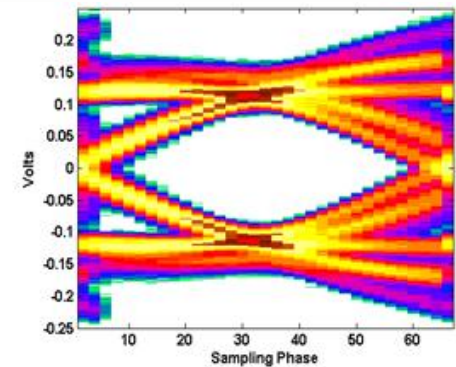# Impact on Signal Integrity

- Let's now zoom into the area around 1.4M to 1.8M bits so that we have a window of 400K bits. We will plot four eye diagrams with bits overlapping,
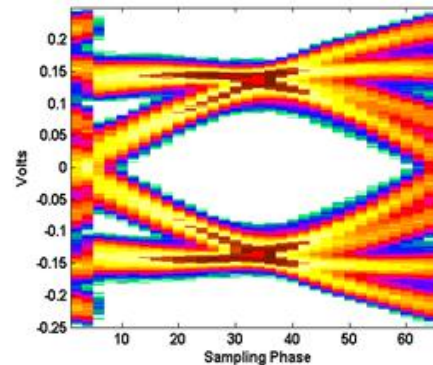

- Before and after transition (a & d), the eyes are cleaner.

- During transitions (b & c) relative moving between clock and data, resulting in slight eye degradation.

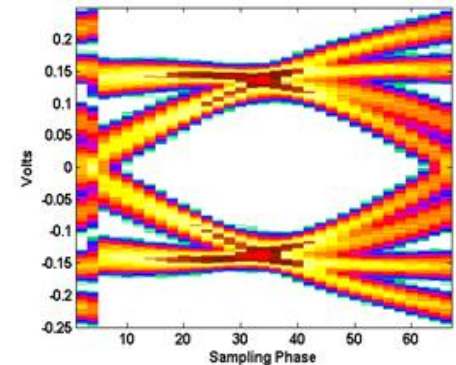- The increased Boost is clearly visible.
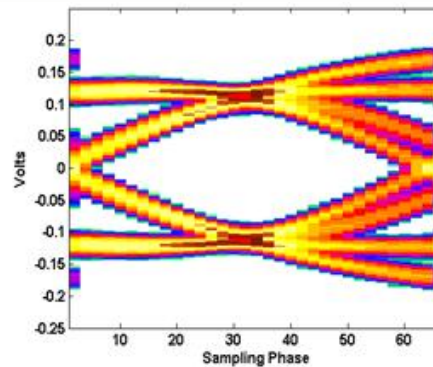
Conclusions

- We have presented the basic concepts of static simulation and dynamic simulation through examples.

- Although static simulation can reveal most problems within a high speed link system, there are situations in which dynamic modeling can do more.

- The downside of dynamic simulation is its longer simulation time. A good planning prior to simulation is very important to achieve what is desired.

- Dynamic modeling can be applied to IBIS-AMI without much effort.