Comprehensive Full-Chip Methodology To Verify Electro-Migration and Dynamic Voltage Drop On High Performance FPGA Designs In The 20nm Technology

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XILINX.
ANSYS® Apache
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UBM Tech

About Xilinx

- Xilinx makes FPGA chips.
  - Successful tape-out at 20nm.
  - The Xilinx design is a mosaic of functional tiles.
    - For example: RAM tiles, programmable logic tiles, IO tiles, etc.
    - Design mix is dominated by custom designs of moderate size.
  - We are limited by vector generation:
    - A complete vector set is generally unavailable.
    - Vectors come in late in the design cycle.
    - Designers often use manually generated, functional vectors.
    - Most vectors are of limited duration.
    - Long vectors result in long runtimes.

Totem Power EM-IR Flows
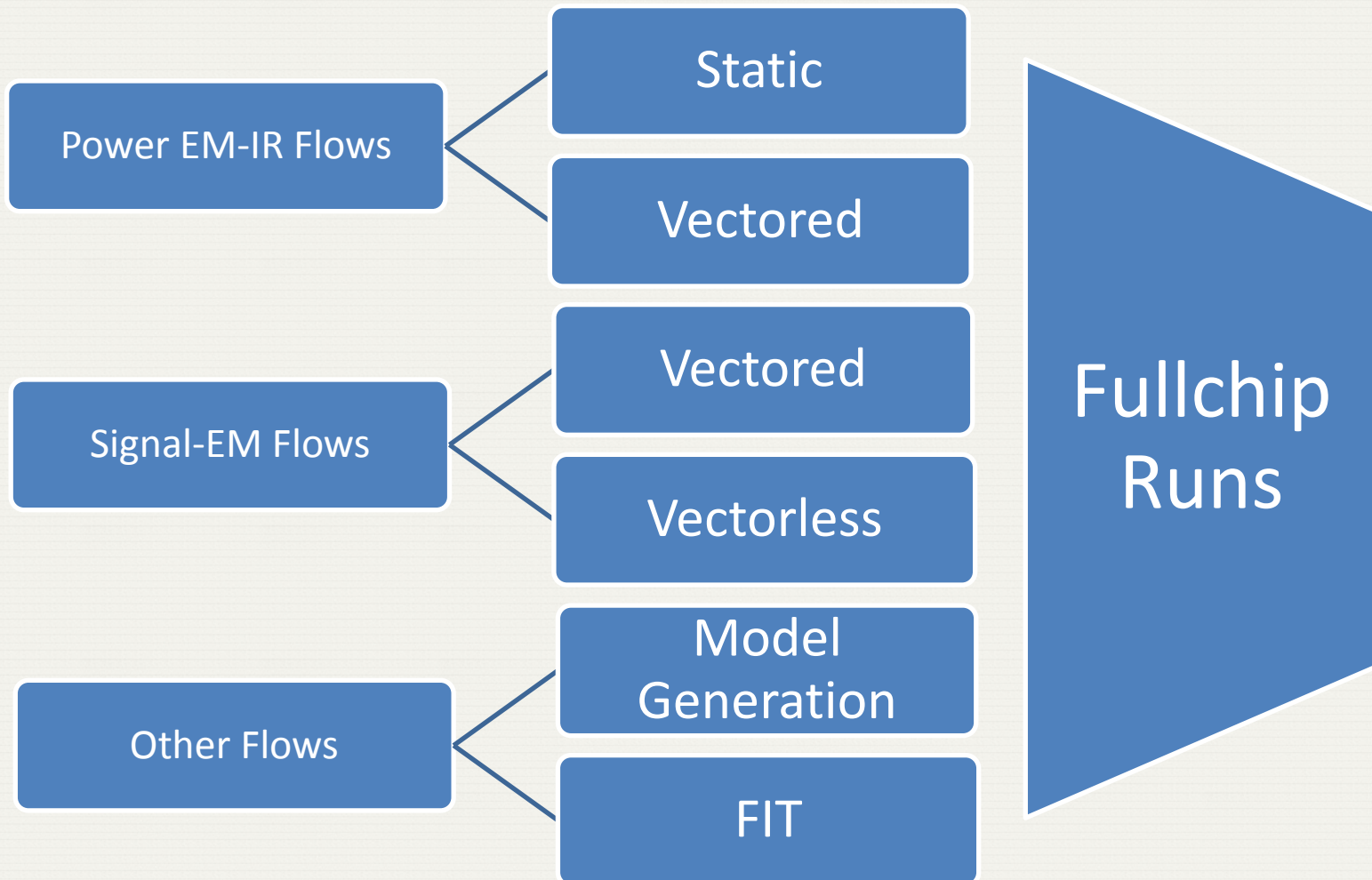
Xilinx EM-IR Philosophy

- We must have 100% coverage:
- We must have "acceptable" accuracy:
    - Accuracy must be "within acceptable bounds" for all design styles.
    - Results must trend as per user intuition.
- Default methodology must never be optimistic.
    - Methodology/tool limitations may cause inaccuracy in result.
    - This inaccuracy must always be "bounded and pessimistic".
- We must have user overrides to overcome limitations of default methodology and accuracy.
- Signal-EM penalty is paid for within a fixed time interval.
    - EM result should <u>not</u> depend on the number of transitions in vector.
    - User overrides for activity factor are allowed.
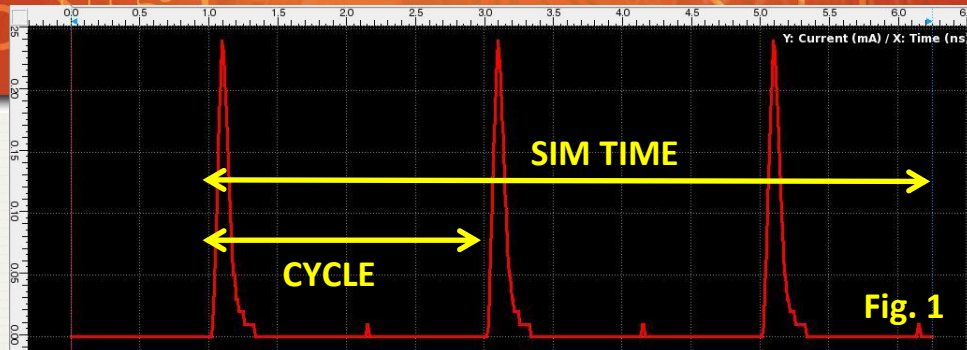
Signal-EM Dependence On Vector *

Fig. 1

Fig. 2

Fig. 3

SIM TIME

CYCLE

Time	Iavg	Irms
Cycle	12uA	42uA
SimTime	12uA	42uA

Fig.1 - For clock nets, AVG and RMS currents match for CYCLE and SIM time.
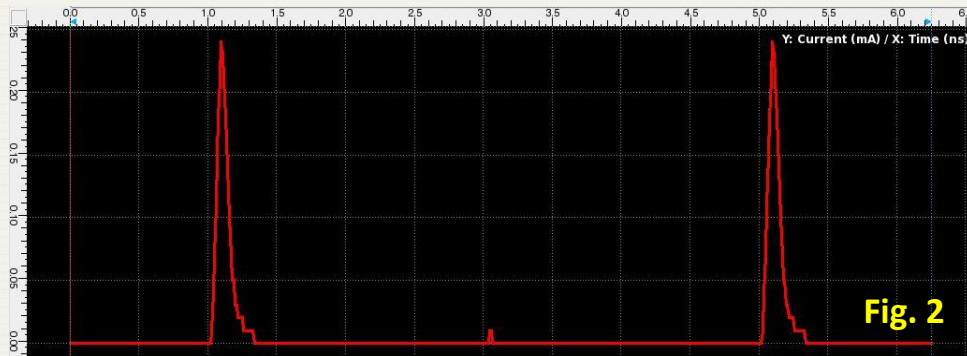
Time	Iavg	Irms
Cycle	12uA	42uA
SimTime	9.2uA	37uA

Fig 2 & 3 - For data nets, AVG and RMS currents depend on the number of transitions in any given time interval.
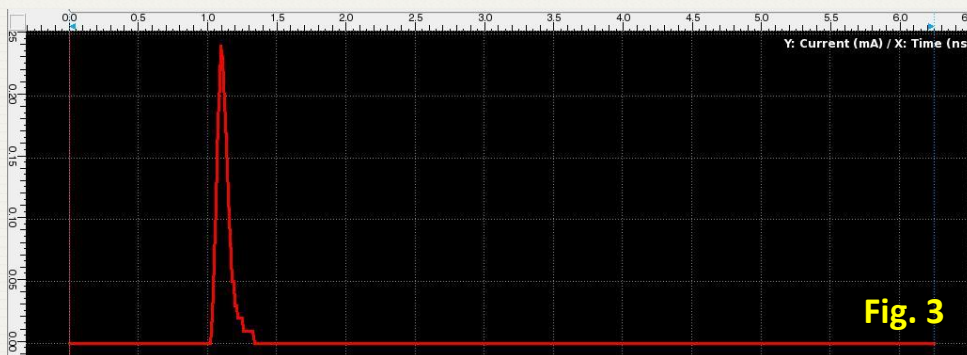
Time	Iavg	Irms
Cycle	12uA	42uA
SimTime	3.8uA	24.3uA

* Inverter testcase, constant load; current values are for PMOS device of inverter.

Window Slicing For EM Computation

> **The idea is to pay the EM penalty within a fixed time period of one cycle.**

- Let's say you have a four cycle simulation (CYCLE1 to CYCLE4)
- Initial delay is 2ns, and each subsequent cycle is 2ns wide.

Simulation Settings:

FREQ	500e06
DYNAMIC_SIMULATION_TIME	8n
DYNAMIC_TIME_STEP	10p

Cycle Definitions:

CYCLE1 " " " " 2ns 4ns

CYCLE2 " " " " 4ns 6ns

CYCLE3 " " " " 6ns 8ns

CYCLE4 " " " " 8ns 10ns
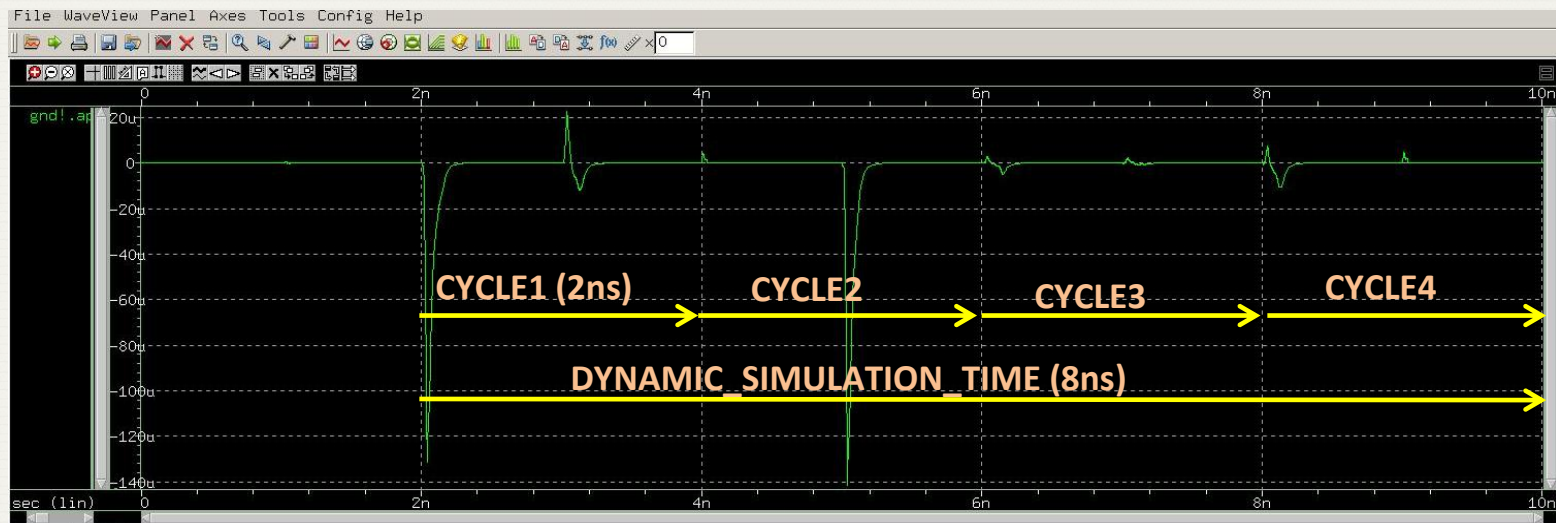
Xilinx EM-IR Requirement

- All designs must pass the following checks:

Flow	Must Pass	Coverage	What Is Checked?
Static	IR / AVG-EM	100%	PG gross-checker on all designs
Dynamic	IR / AVG-EM / RMS-EM	<100%	Large drivers / Large arrays Decap check / Jitter Concerns
Signal-EM	AVG-EM / RMS-EM	100%	Mixed-Mode Signal-EM enables 100% coverage

- Level at which EM-IR is run must capture context adequately:
  - Design size must be large enough, comparable to bump pitch.
  - Design must comprise upper metal layers, must include decaps, etc.
- EM result must be independent of the quality of vectors.
  - By default, clock nets are analyzed at TR=2, while non-clock nets at TR=1.
- Design must pass FIT.
 - AVG-EM violations can be waived if design passes FIT.

What is FIT?

- FIT stands for "Failure In Time."

- A fullchip FIT of "1" indicates that the <u>failure rate</u> of the part will be 0.1% after 10 years.
  - The fullchip FIT budget is split between AVG EM and TDDB.
  - The fullchip budget is divided into subblock budgets.

- Subblock FIT budget depends on:
  - Area of the subblock
  - Frequency of the subblock
  - Design Style
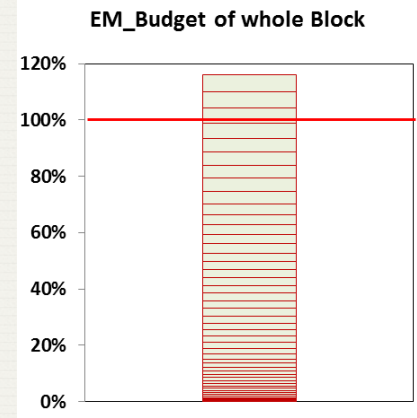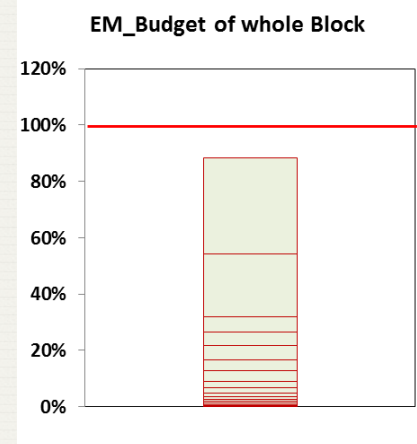
FIT-Based EM Check versus Rule-Based EM Check

- *Budget* represents how much design is *allowed* to contribute to Product Failure Rate (FIT)

I/Imax from EM Tool
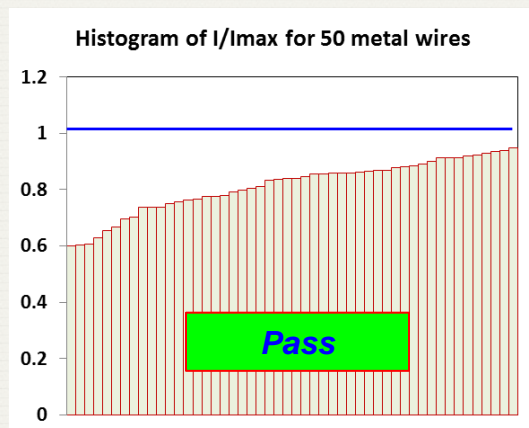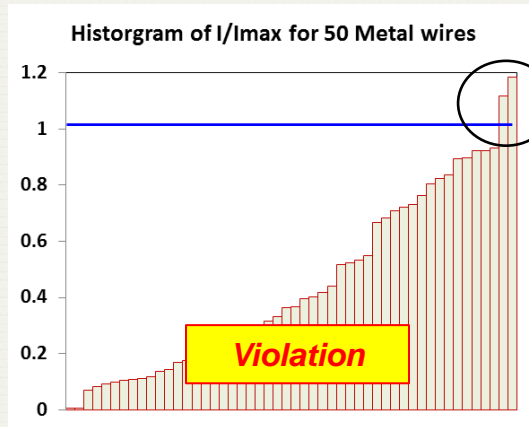
FIT Comparison

- **Rule-based check might be too conservative (top) or overlook actual risk (bottom).**

EM-IR Corner Methodology

- The EM-IR corner is:
  - Fast Transistors
  - High Temperature
  - Extraction is Typical
  - Nominal Supply voltages
- EM-IR corner must match:
  - Power Corner
  - Timing Corner
  - SPICE corner for spice simulations

# Power EM-IR: Modes Of Operation

- Transistor-level Power EM-IR flows can be run in two modes:
  - Static:
    - Power is distributed over all transistors in the design.
    - Transistor current is assigned as below:

$$I_{transistor} = \frac{P_{\sup}}{V_{\sup}} * \frac{W_{transistor}}{\sum W_{transistor}}$$
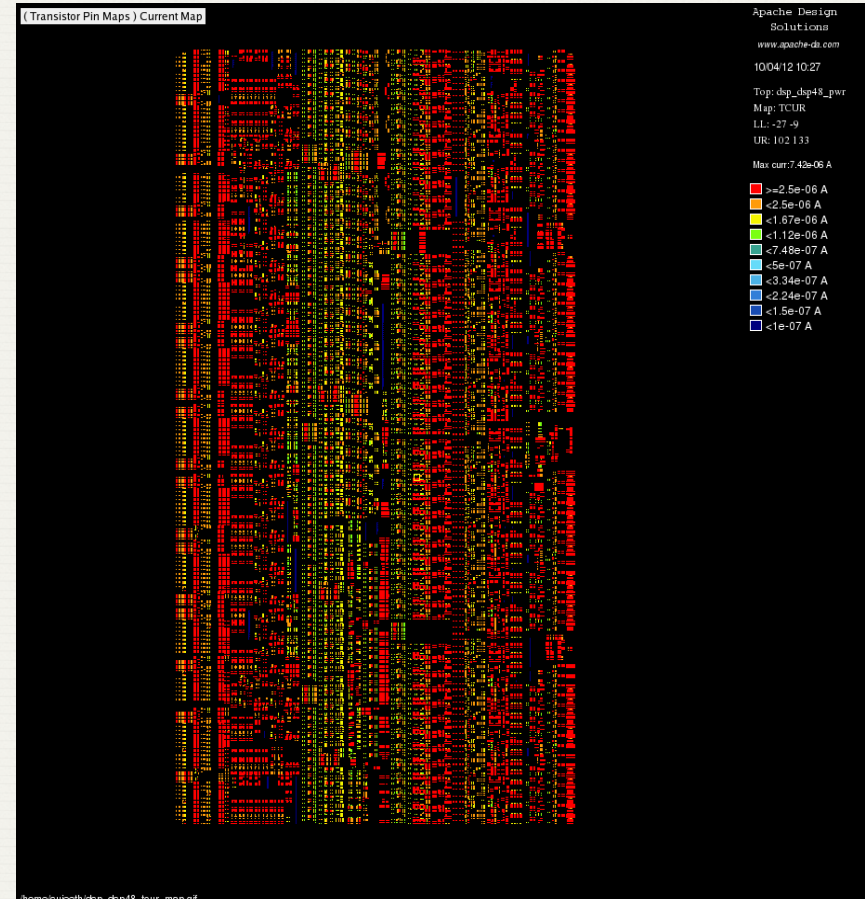
  - The Static check is a gross-checker, but it gives 100% coverage.
  - Dynamic (Vectored)
    - Only the active/switching areas of the design get any current assignment.
    - All transistor currents are probed through a SPICE simulation.
    - The Dynamic check is accurate, but gives limited coverage.

Device Current Distribution: Static vs. Dynamic

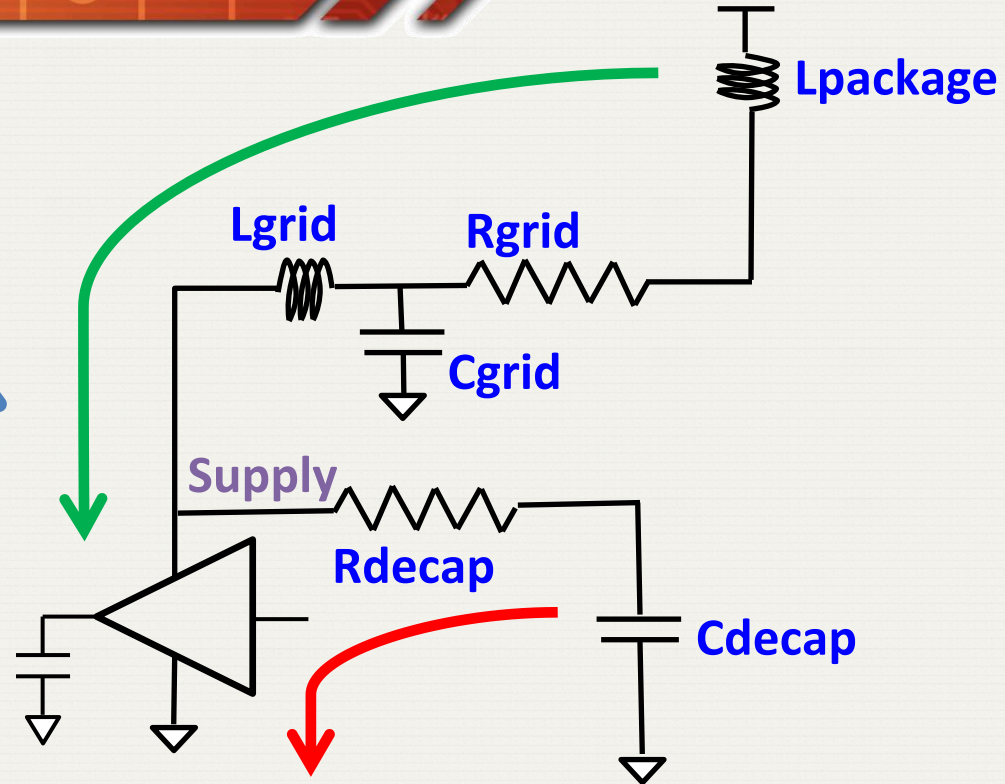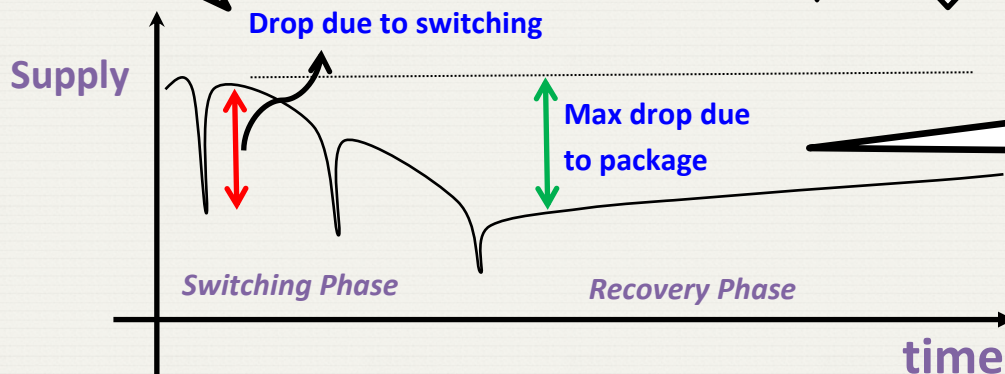**Dynamic**
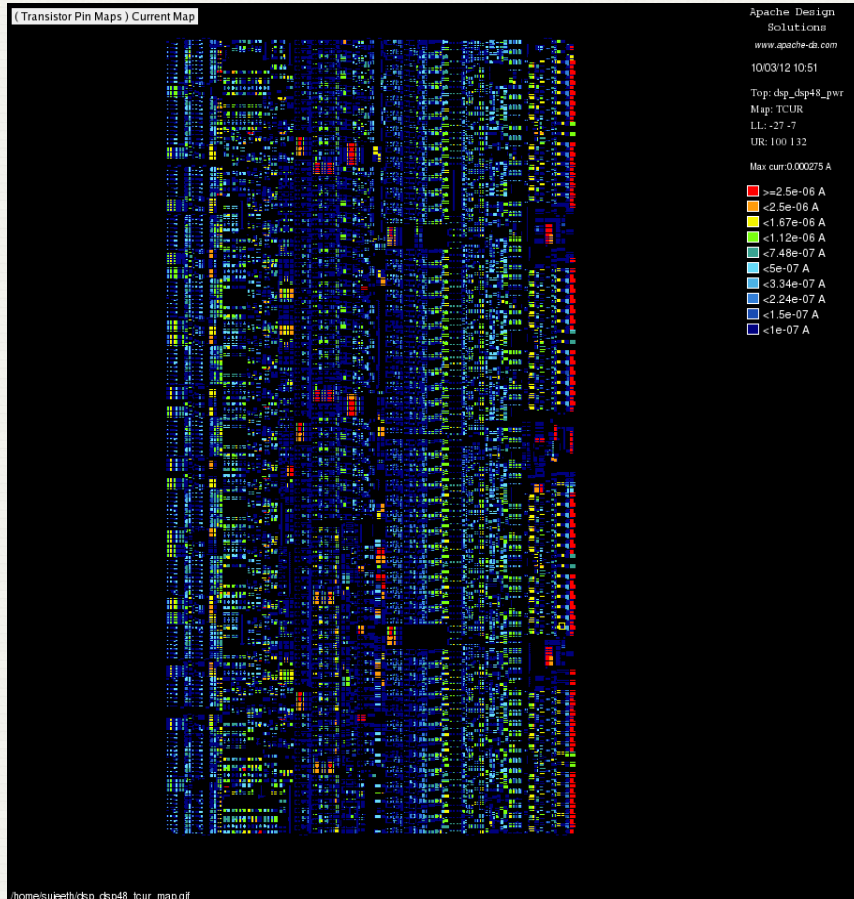
Static

Total power in both cases was the same,

Dynamic Drop - Decap Efficiency Test
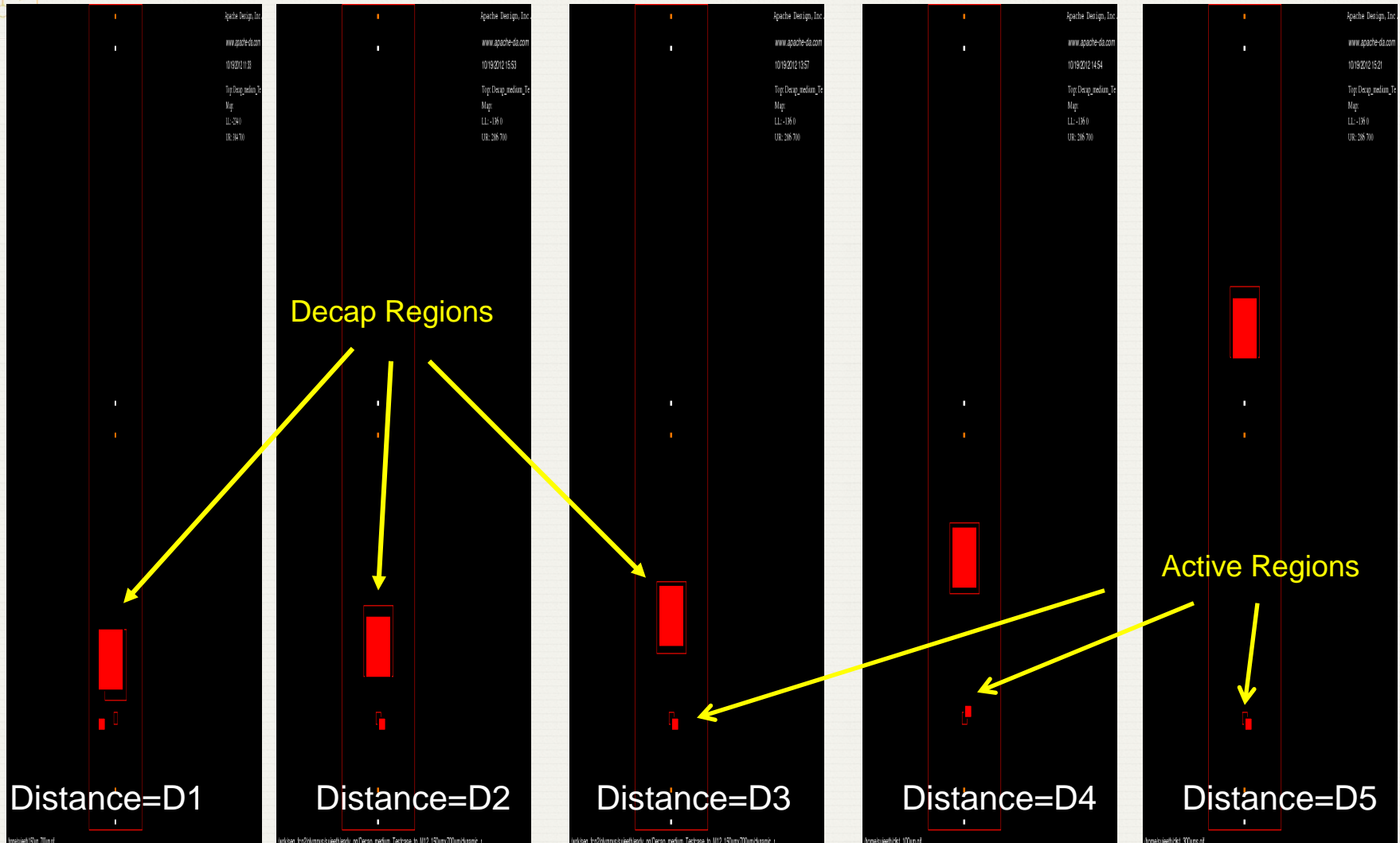
This simulation tests the following:

Location of power noise sources, distance to sensitive circuitry, amount of DvD noise, effect of decap on DvD, etc.

Lpackage

Lgrid

Rgrid

Cgrid

Supply

Rdecap

Cdecap

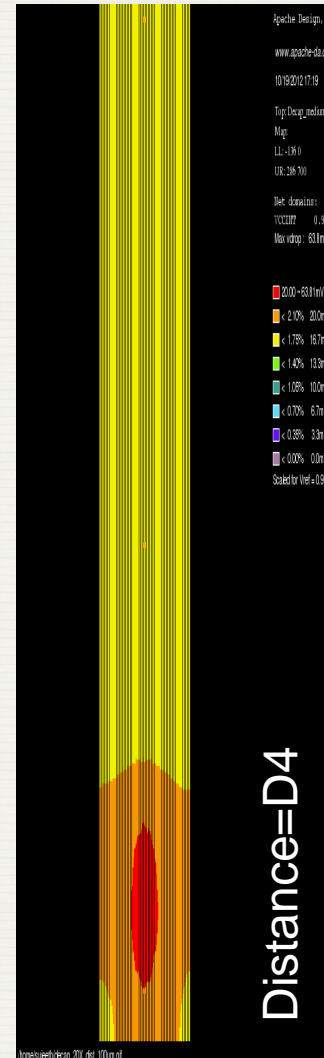The purpose of Dynamic Analysis is to measure this.

A very long simulation will end up measuring this.

Drop due to switching

Supply

Max drop due to package

Switching Phase

Recovery Phase

time

Dynamic Drop - Distance Of Decap

Decap Regions

Active Regions

Distance=D1 Distance=D2 Distance=D3 Distance=D4 Distance=D5

Dynamic Drop - Distance Of Decap

Distance=D1

Distance=D2

Distance=D3

Distance=D4
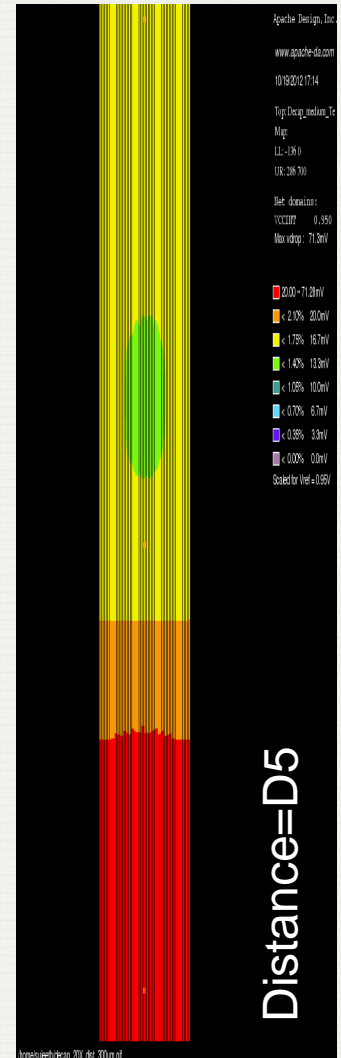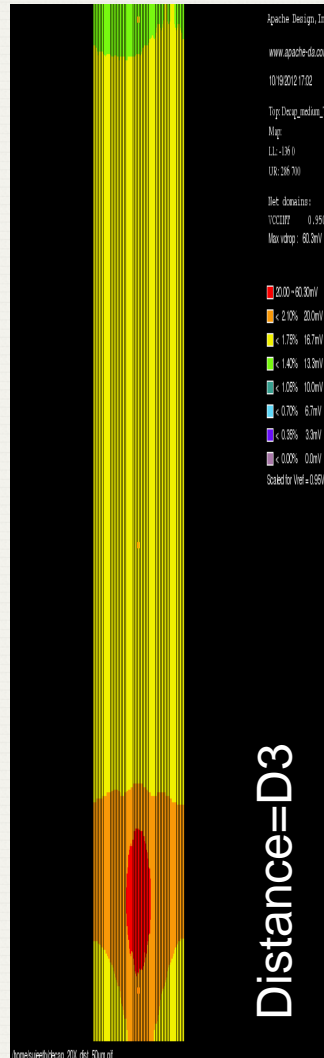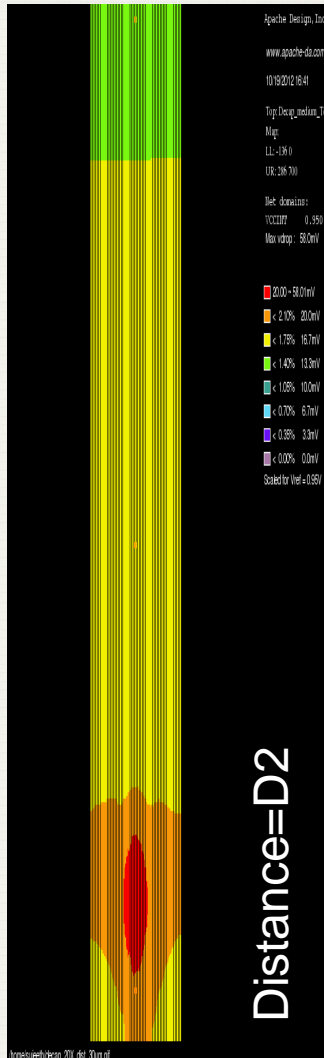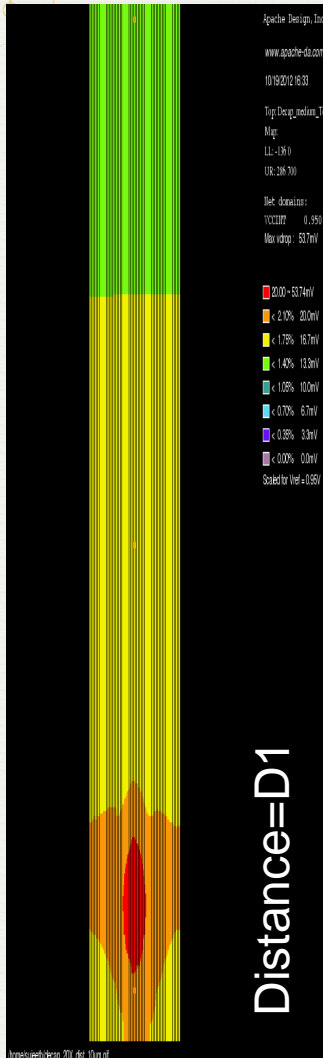
Distance=D5

Decap Placement Recommendation

Dynamic Power Noise Improvement

Legend:
- 30%-40%
- 20%-30%
- 10%-20%
- 0%-10%

Axes: Decap to Driver Ratio (R1–R5), Decap Distance to Driver (D0–D5)

Desired Solution Space
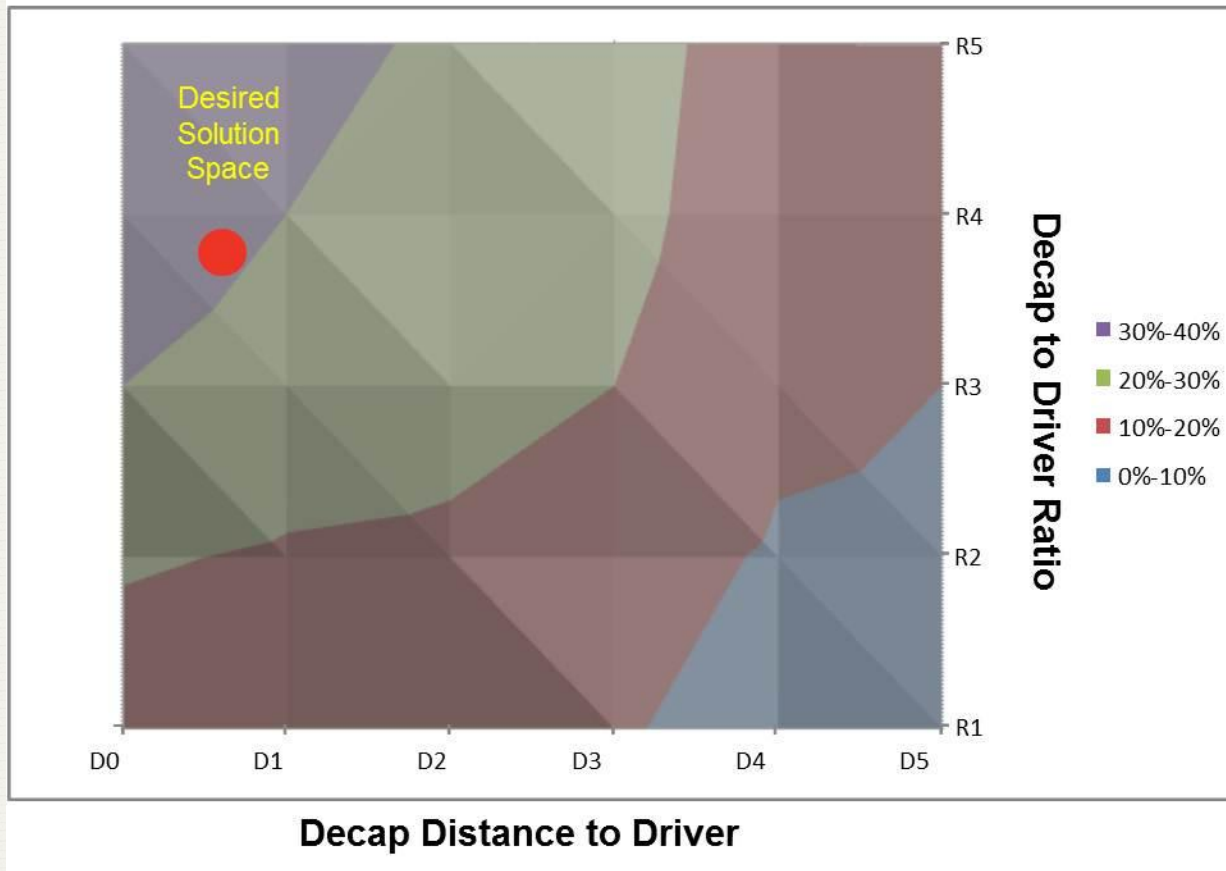
D is distance: D5 >> D4 >> D3 >> D2 >> D1

R is decap ratio: R5 >> R4 >> R3 >> R2 >> R1

Power Delivery System Overview
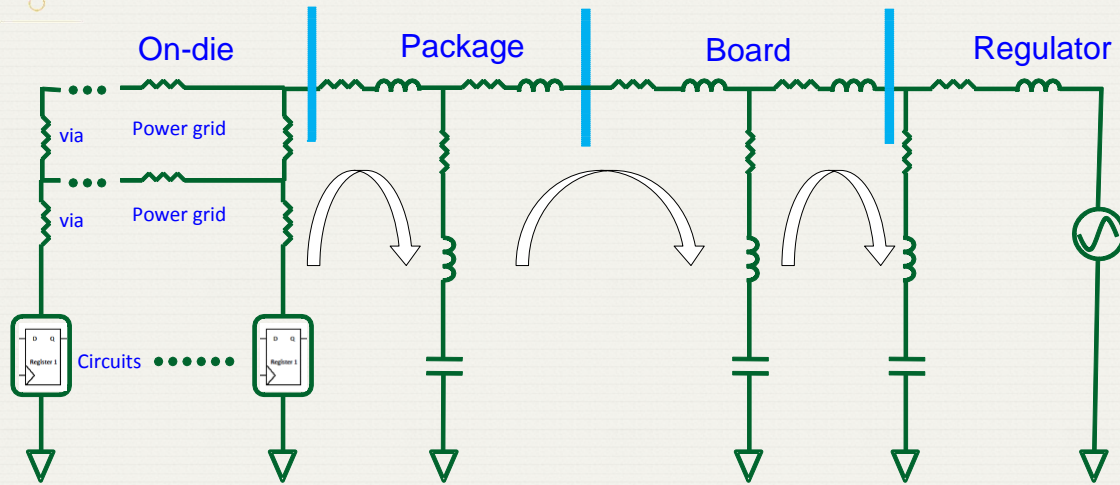
IR Drop Limit – Static vs. Dynamic
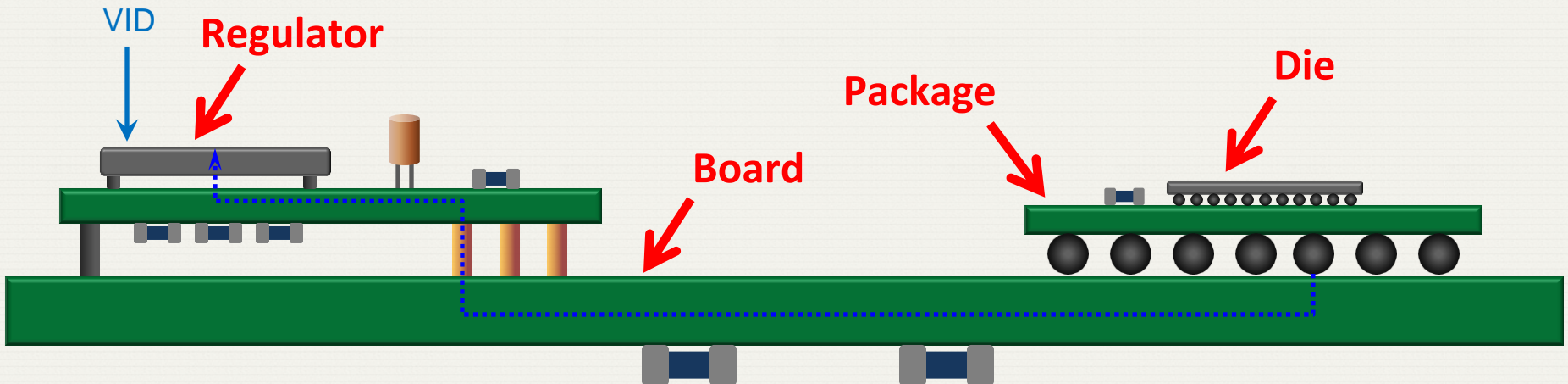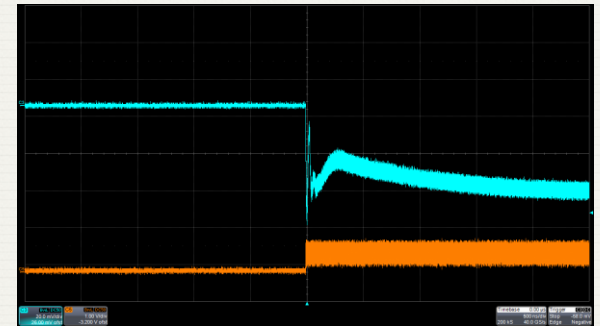
- Components of IR drop:
  - Package Drop
  - On-die Drop

- How to arrive at a Static IR limit?
  - An arbitrary low number!
  - Average drop over time – average drop from a worst case scenario.
  - Static Limit can match DC offset used in timing characterization.

- How to arrive at a Dynamic IR limit?
  - Timing characterization
  - Clock Jitter simulations
  - Pay attention to large drivers and sensitive circuitry
  - Total IR drop budget is split between off-die and on-die IR drop
  - Simulations include package inductor model

EM Budgeting / Failure Mechanisms

- Safety margins are built in:
  - Process/Fab Margin
  - Design Margin

- Failure Mechanisms in EM:
  - AVG EM limit is linked to metal voids.
  - RMS EM limit is linked to heating.
  - Heating causes further drop in AVG EM limit.

- Unidirectional / bidirectional segments:
  - Unidirectional more susceptible to AVG EM failures
  - Bi-directional more susceptible to RMS failures

- Poly/Metal Resistor Instances and Inductors:
  - Resistor instance paths are not valid candidates for the IR drop limit rules.
  - We "break" these paths so IR analysis is done up to the first resistor or inductor instance only and EM analysis is done on the internal path.

Why We Should Model Heat Flow

Increases temperature

Reduces AVG EM Limit

Bidir wires susceptible

Unidir wires susceptible

Generational Increase in RMS current

More EM violations
Less Design Margin

Generational increase in Slew/Fanouts

Less design margin

20nm Process Node

Increased wire density

More design margin

Less EM violations
More Design Margin

Better heat dissipation

Leverage FIT

Drive current drops with higher temperature

Vectorless Signal-EM – Driver Current Profiles

Uni-dir current

Bi-dir current

Tcycle

Slew

Signal Voltage

Time

Switching Current(bi-directional)

Signal Current

Time
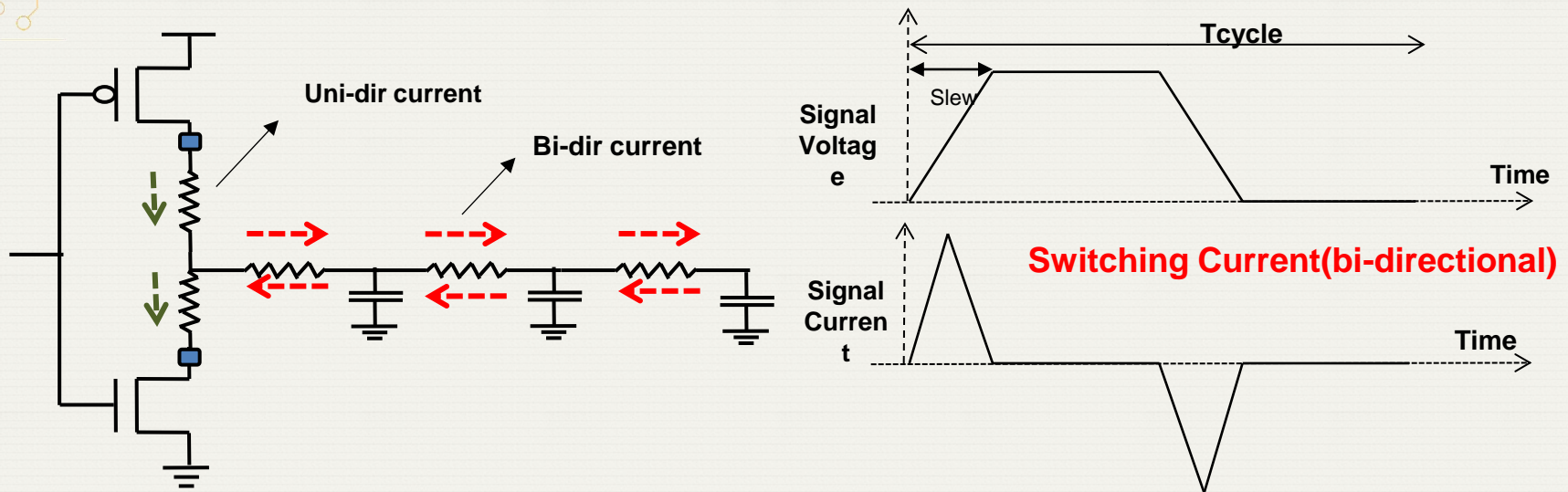
```
Isw(bidir)  = F(Cload, Vdd, Slew)
Icrowbar(unidir) = SF* Isw
SF□ user specified scaling factor
```

```
Iavg = Iavg(1cyc) * TR*Freq
Irms = Irms(1cyc)*TR*Freq
Ipeak = Ipeak(waveform)
```

- **Single cycle simulation will be performed(1charge,1discharge) for different frequency domains.**

- **Uni-directional current(crowbar) will be scaled during post-processing (w/o simulation).**

- **Toggle rate will be used for Iavg/Irms computation only (not for constructing current waveforms).**

Vectorless / Mixed-Mode Signal-EM

- Vectorless gives 100% coverage!
  - Default values are set to be aggressive.

- Results scale with frequency, slew rate and toggle rate.
  - Assuming the following reference EM settings:
    - Frequency □f1; Slew □slew1; Load □load1; Toggle Rate □TR1
  - Assuming the following DUT settings:
    - Frequency □f1; Slew □slew1; Load □load1; Toggle Rate □TR2

| EM Scaling with Electrical Parameters	AVG	RMS
Frequency	f2/f1	Sqrt (f2/f1)
Slew	No change	Sqrt (slew2/slew1)
Load	load2/load1	Sqrt (load2/load1)
Toggle Rate	TR2/TR1	?

RMS EM Dependence On Peak Current

> **RMS EM is strongly influenced by peak current.**

– RMS is the SQRT of the average of the square of the current.

	Avg i	Avg i^2	RMS i
Case 1	2	8	2.8
Case 2	2	4	2
Case 1 @ half TR	1	4	2
Case 2 @ half TR	1	2	1.4

Higher peak causes higher RMS current for same total charge*.

Halving of the TR reduces RMS by sqrt (2)
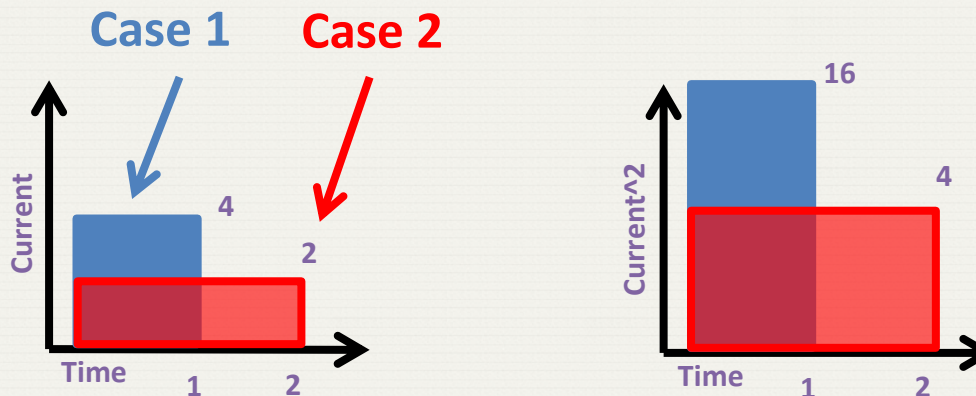
Case 1 *Case 2*

This assumes current profiles are completely enclosed within the same cycle time of 2.
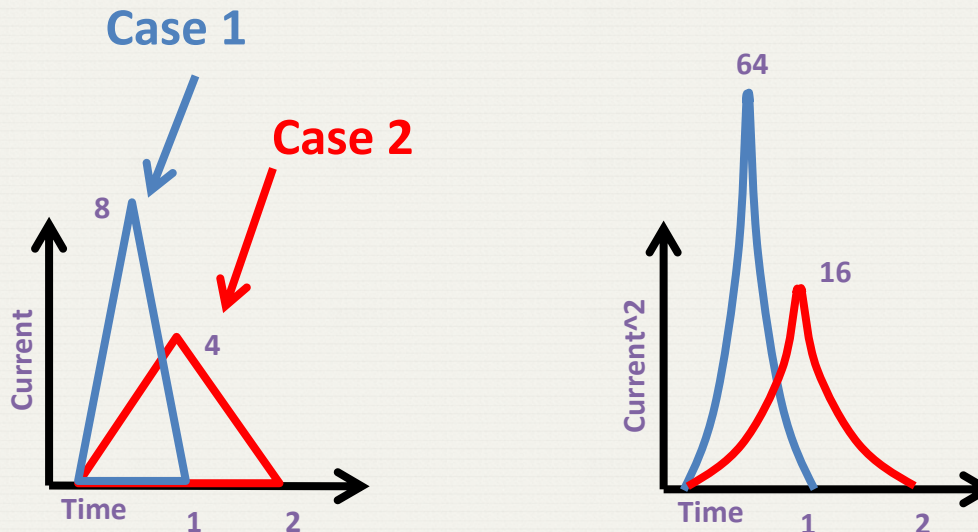
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RMS EM Dependence On Slew Rate

> **RMS EM is strongly influenced by peak current.**

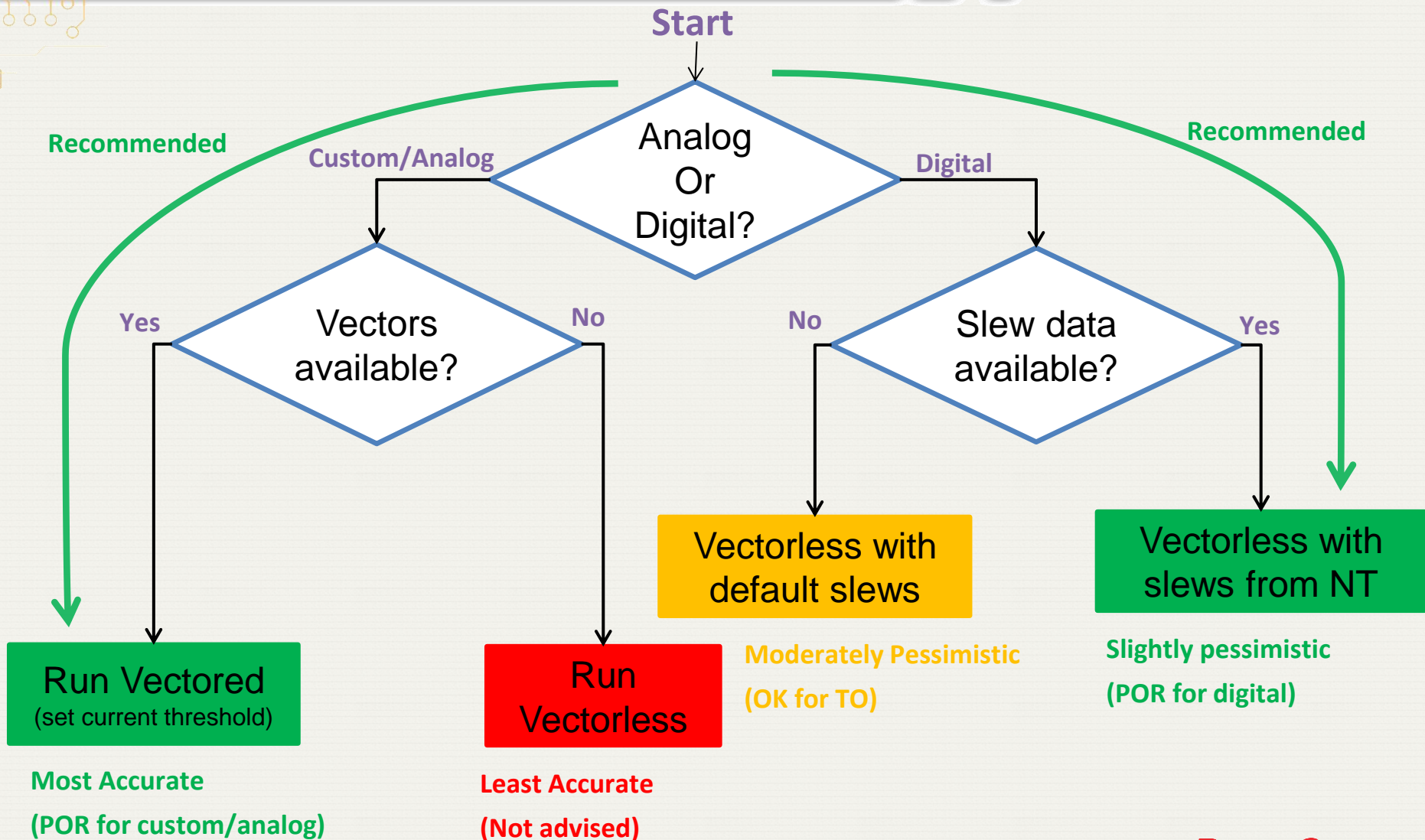– RMS is the SQRT of the average of the square of the current.

	Avg i	Avg i^2	RMS i
Case 1	2	10.6	3.3
Case 2	2	5.3	2.3

Halving of the slew reduces RMS by sqrt (2)

Case 1

Case 2

8

4

Current
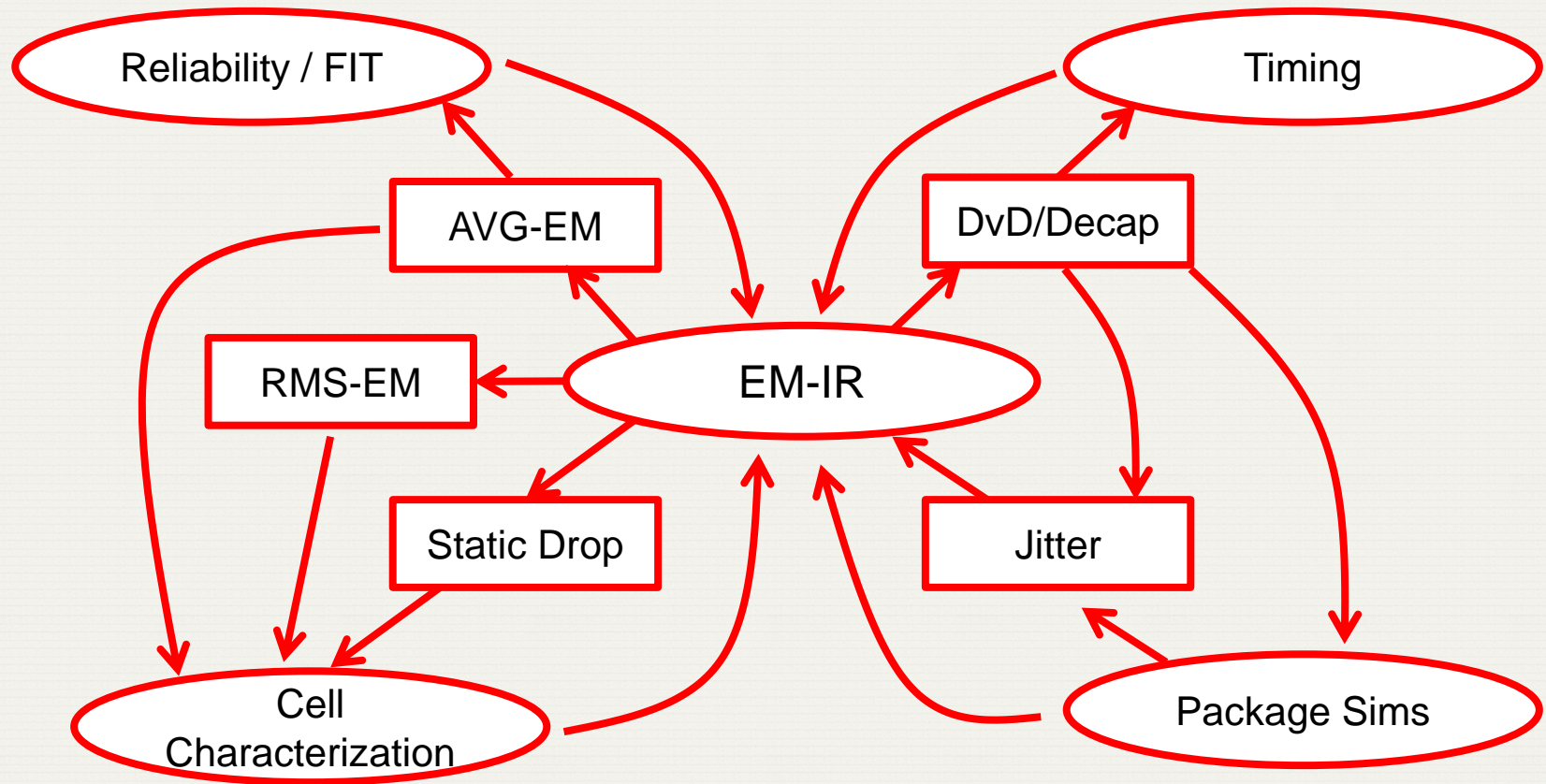
Time

1

2

64

16

Current^2

Time

1

2

* This assumes current profiles are completely enclosed within the same cycle time of 2.

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Should I run Vectored Or Vectorless Signal-EM?

Start

Analog Or Digital?

Custom/Analog → **Vectors available?**

Digital → **Slew data available?**

Recommended (left)

Recommended (right)

Yes → **Run Vectored** (set current threshold)

No → **Run Vectorless**

No → **Vectorless with default slews**

Yes → **Vectorless with slews from NT**

Most Accurate (POR for custom/analog)

Least Accurate (Not advised)

Moderately Pessimistic (OK for TO)

Slightly pessimistic (POR for digital)

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How the methodologies are linked…
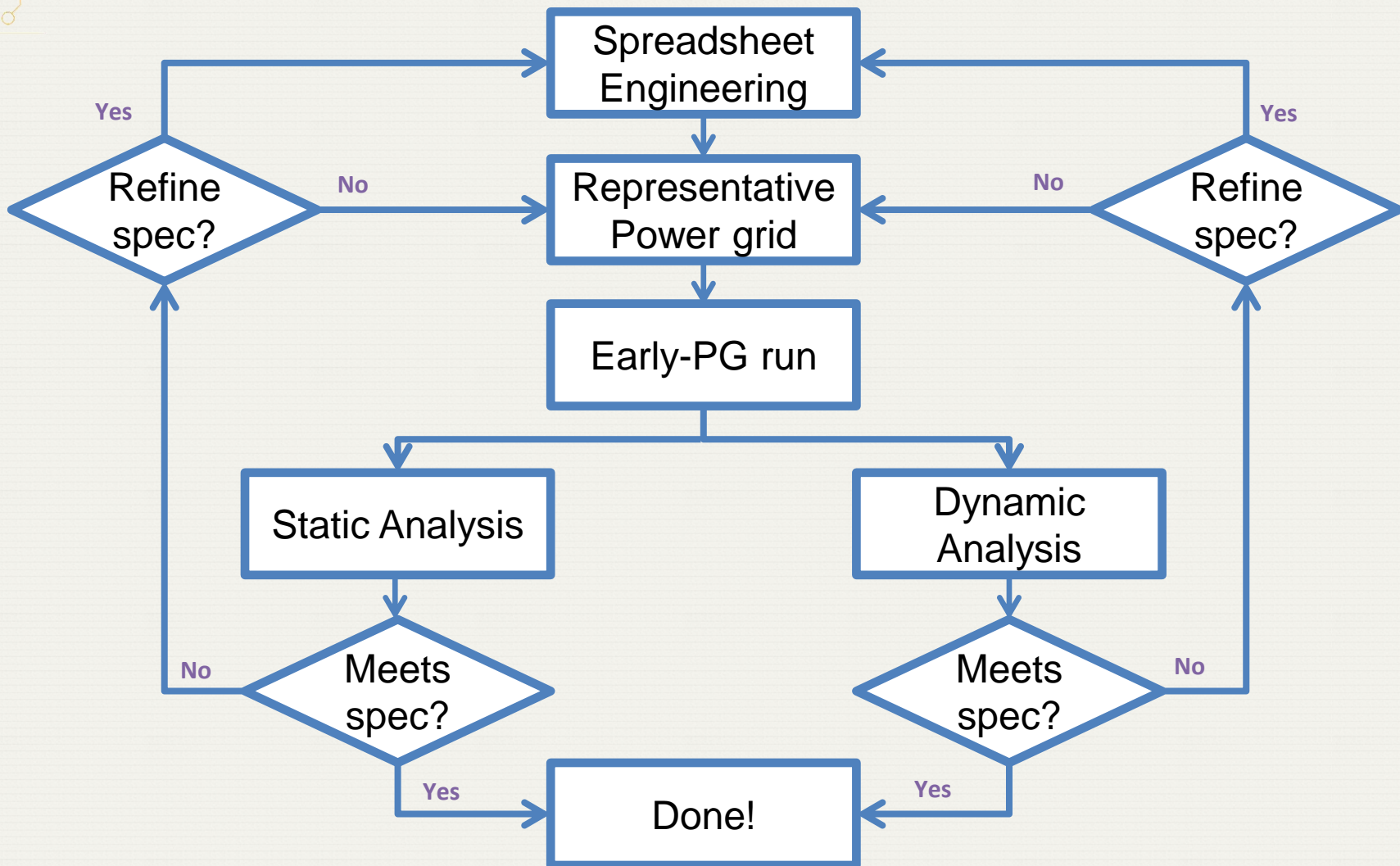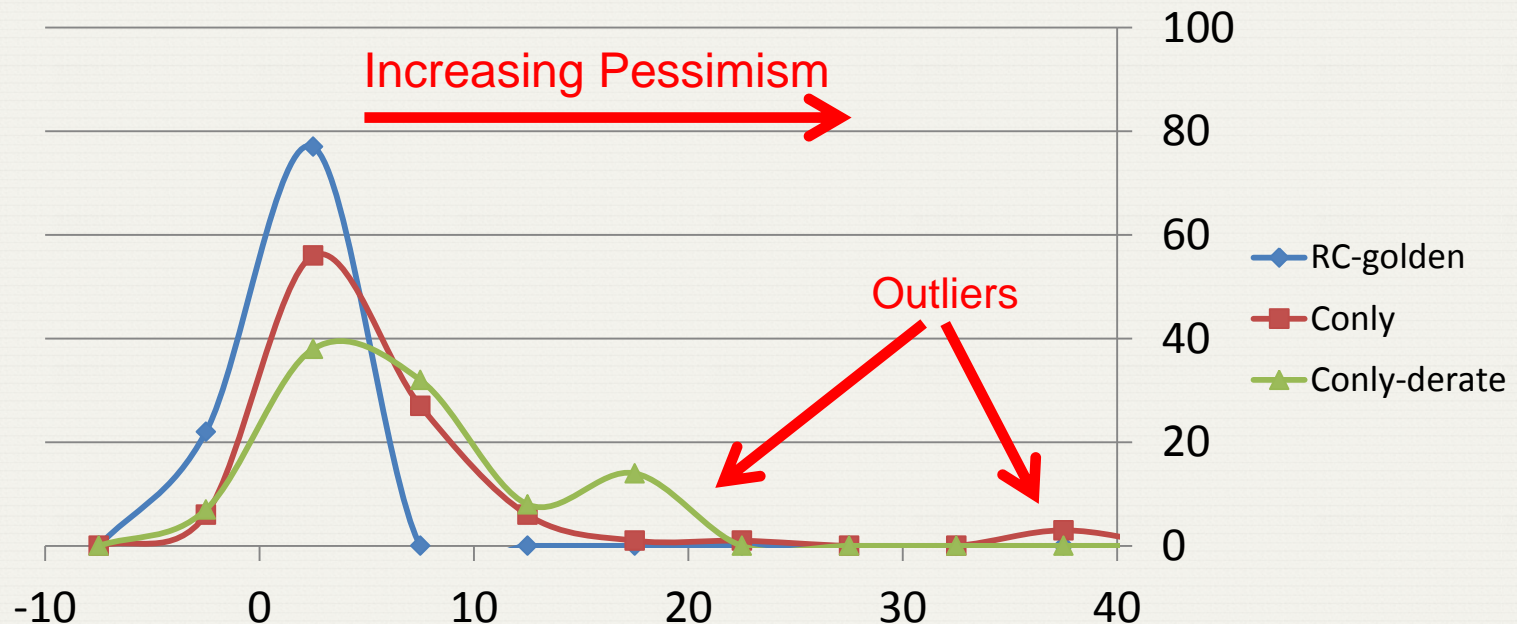
Accuracy – Transistor Level Vectored IR

☐ **Y-axis represents % of the total count of destination device diffusions.**

☐ **X-axis is the accuracy range -10mV to 40mV.**

☐ **Sample size: 10,000 worst transistors from 6 testcases**

☐ **Both analog and digital testcases were considered.**

Accuracy – Transistor Level Vectored Signal-EM

☑ **Y-axis is normalized to %.**

☐ **X-axis is the accuracy range -50% to +50%.**

☐ **Sample size small ~ 200 nets**

☐ **Both analog and digital blocks were considered.**
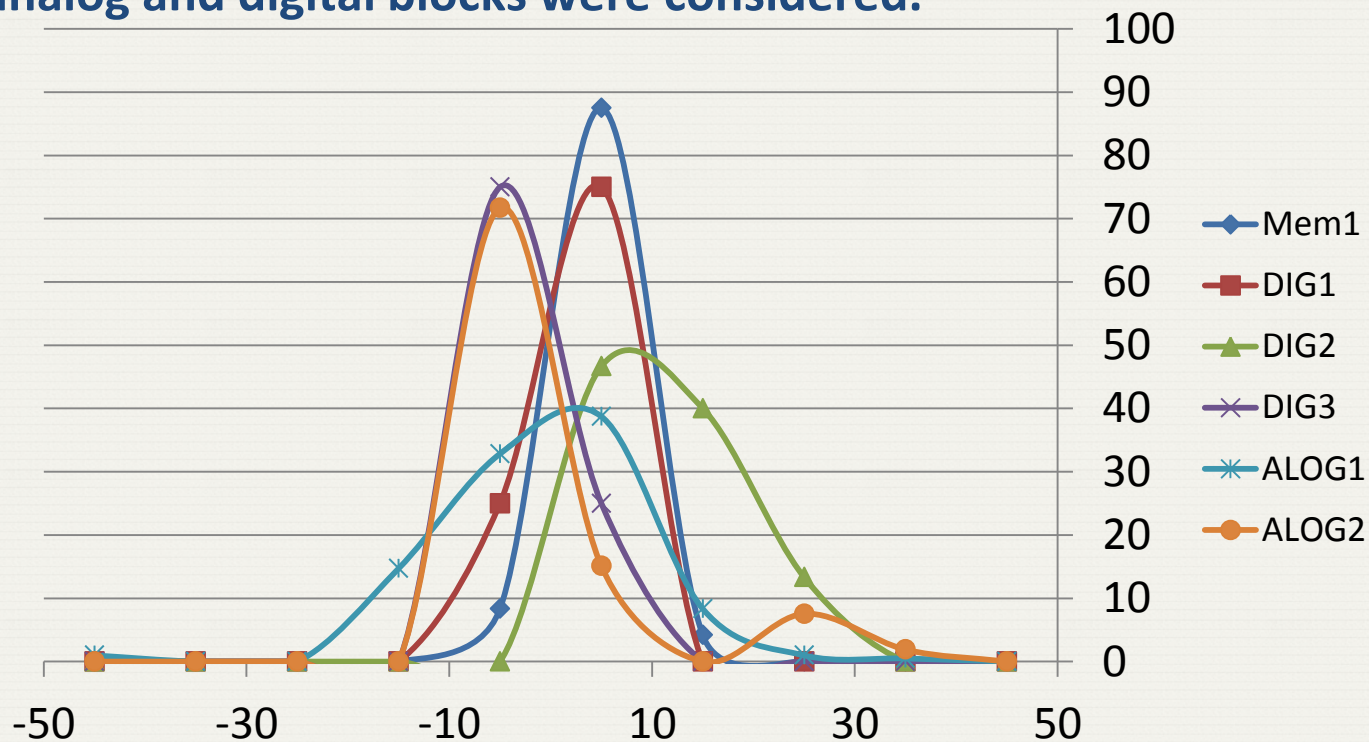
Various Design Styles

- Our EM-IR Tools:
  - Totem ☐For transistor level designs
  - Redhawk ☐For cell based designs
- We will have the following design styles:
  - PNR Blocks
  - Custom Blocks
  - Mixed Blocks (Custom + PNR blocks)
- Blocks come in different sizes:
  - Medium (no capacity issues)
  - Big (possible capacity issues)
- Levels of Hierarchy / Analysis:
  - Block level
  - Subblock level
  - Arbitrary level (for exceptional cases)
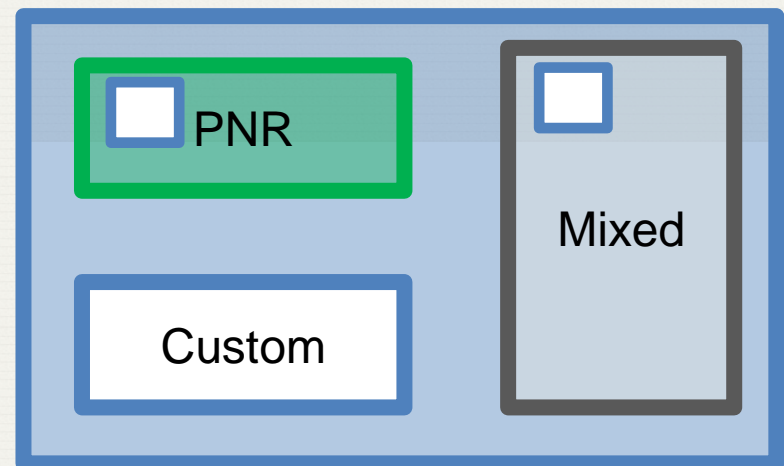
Fullchip Partitioning

➤ A high level view of fullchip:
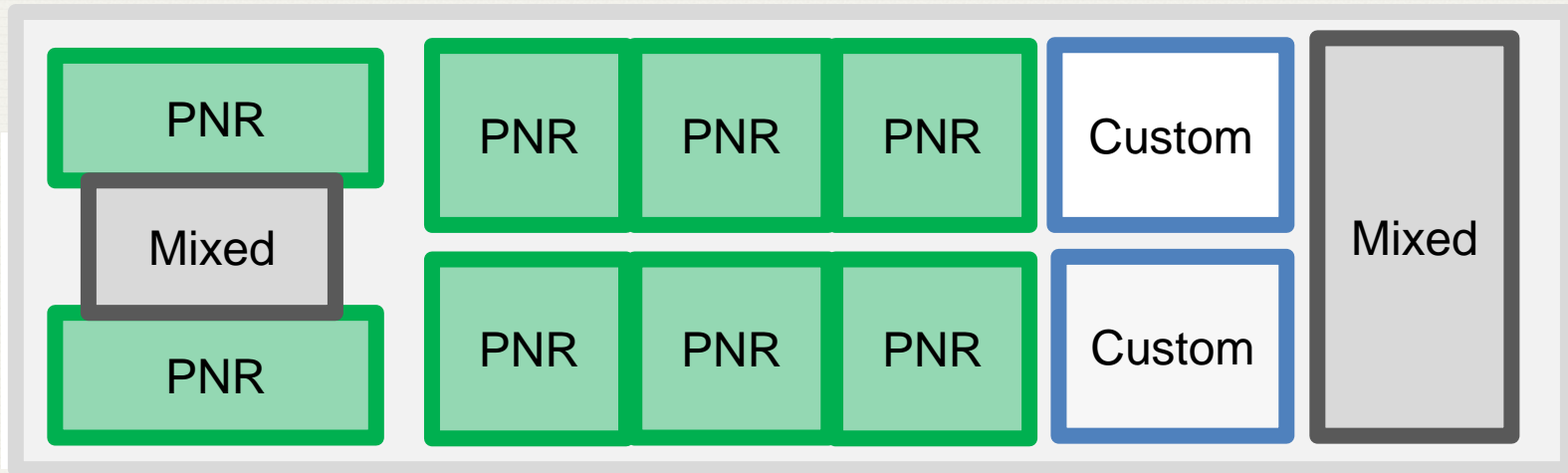
- Anatomy of a "Mixed" block:

  - ☐ **Lib/Macro/Custom**

  - ☐ **PNR Boundary**

Design Styles And Tool Considerations

- Common Design Styles:

Type	Flow	Comments
Standard Cell	Cell Level	Can't do FIT
Custom	Transistor level	100% coverage
Mixed Blocks	Cell and/or Transistor Level	Some coverage loss

- Size Considerations:

Size	Runtime*	Cell Flow	Transistor Flow
Small	3 hours ?	1 million instances	0.3 million transistors
Medium	1-2 days	n/a	1 million transistors
Large	2-4 days	n/a	2+ million transistors

* This excludes SPICE run time. Assumes dedicated machine.

"Divide And Conquer" Approach

- How to break hierarchies?
  - Level of analysis must be considered early in design cycle.
  - Choice of subblock hierarchy impacts fullchip analysis.
  - Poor planning results in loss of coverage and loss of accuracy.

- Recommendations:
  - Fullchip analysis should traverse down to level of subblock analysis.
  - Subblock models must be propagated to fullchip analysis.

| Required To Run	At Level	Flow	Comments
Static and Dynamic Power EM-IR	Block level	Transistor	
AVG and RMS Signal-EM	Block level	Transistor	Run Vectorless Signal-EM
Static and Dynamic Power EM-IR AVG and RMS Signal-EM	Custom Cell	Transistor	Follow directions for "Custom" blocks

Design Types And Flow Styles

BLOCK TYPE	ANALYSIS	BLOCK DYNAMIC	
		Vectored	Vectorless
Custom	Power EM/IR	Transistor Level Vectored	
	Signal EM	Transistor Level Analog ☐Vectored/Mix-Mode Digital ☐Vectorless	
P&R	Power EM/IR	Cell Level Vectorless	
	Signal EM	Cell Level Vectorless	

Package Simulations With On-Die Models
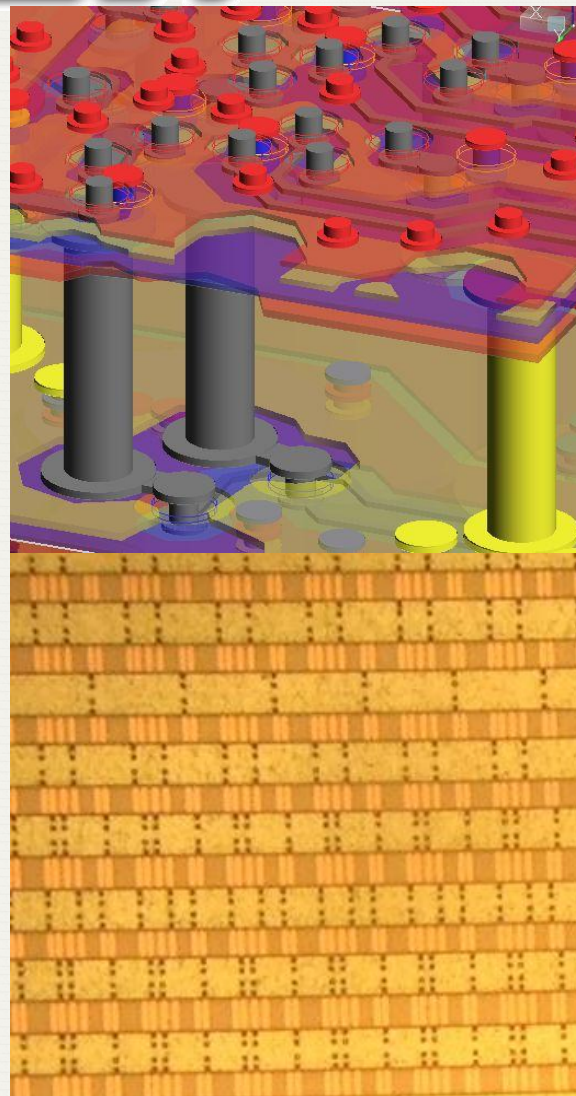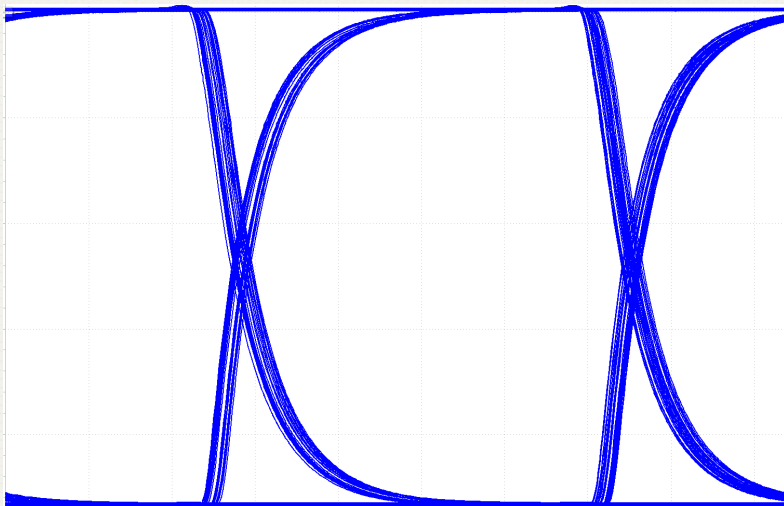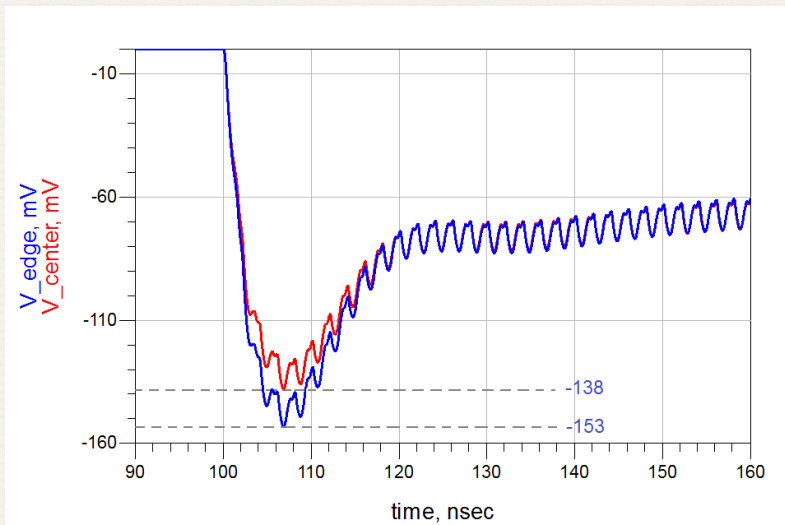
Interposer Simulations

- Interposers:
  - Stand-alone run
  - Static Simulation
  - Very low IR budget allowed
  - Must fix AVG EM
  - Regional power assignments

(Voltage Drop Maps) Wire and Via
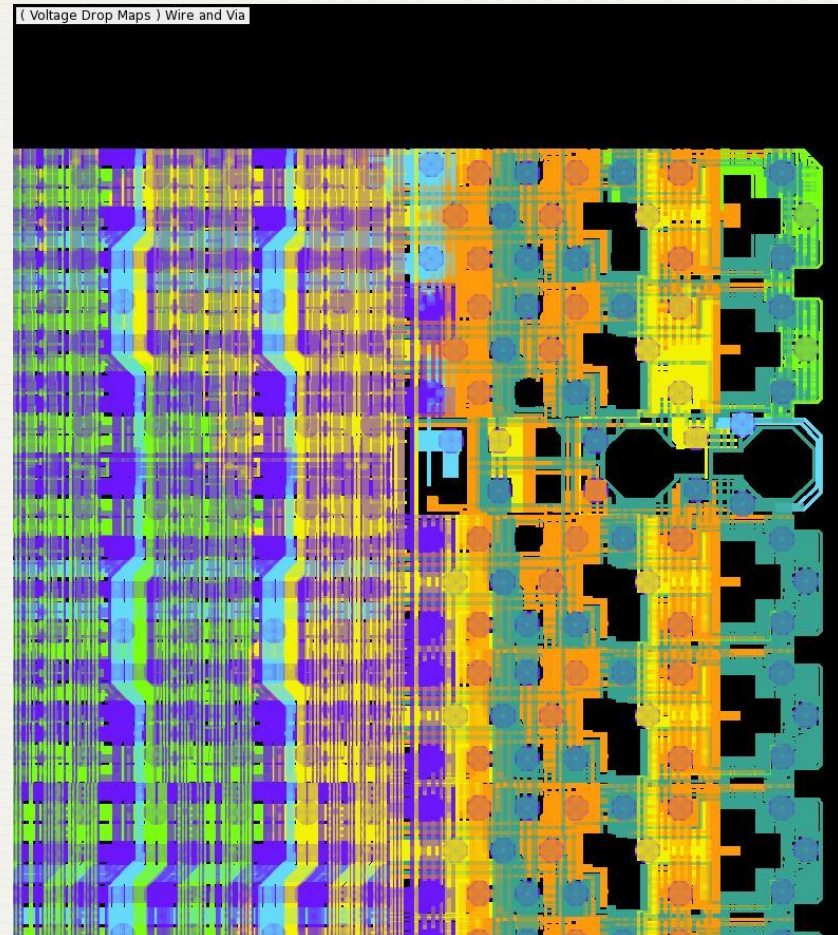
Summary

- ## Highlights:
  - We have very high design coverage (~100%).
  - We have very good accuracy.
  - Default methodology is conservative.
  - EM-IR methodology has withstood the scrutiny of the design community.

- ## Areas Of Improvement:
  - Handling super large designs (capacity and runtime)
  - Managing hierarchy / Integrating multiple runs to analyze in-between metal
  - Hierarchical FIT

Thank You!